Load-Line Regulation With Estimated Load-Current Feedforward: Application to Microprocessor Voltage Regulators

Angel V. Peterchev, *Member, IEEE*, and Seth R. Sanders, *Member, IEEE*

***Abstract*—A consistent framework for load-line regulation design is presented, applicable to microprocessor voltage regulators (VRs) using either electrolytic or ceramic output capacitors. With conventional feedback control, the loop bandwidth is limited by stability constraints linked to the switching frequency. The output capacitor has to be chosen sufficiently large to meet the stability requirement. Load-current feedforward can extend the useful bandwidth beyond that imposed by feedback stability constraints. With load-current feedforward, the size of the output capacitor can be reduced, since it is determined solely by large-signal and switching-ripple considerations which are shown to be less constraining than the feedback stability requirement. This work points to the feasibility of microprocessor VR implementations using only a small number of ceramic output capacitors, while running at sub-megahertz switching frequencies.**

***Index Terms*—DC–DC power conversion, estimation, feedforward systems, impedance control, load-line, microprocessors, pulsewidth modulated (PWM) power converters, regulators, transient response, voltage control, voltage regulator (VR), voltage regulator module (VRM).**

I. INTRODUCTION

VOLTAGE regulators (VRs)[1] convert 12-V bus voltage to the microprocessor supply rail of about 1.2 V. They have to be able to handle load transients in the range of 100 A, with rise and fall times on the order of tens of nanoseconds. At the same time the output has to be regulated tightly to a load-line with an impedance close to 1 mΩ [2], [3].

The low conversion ratio in VRs presents a challenge since the duty ratio may saturate during large unloading transients, thus slowing down the response. Decreasing the inductor value increases the speed of response, however, this also increases the inductor current ripple and the resulting power loss. On the other hand, if a large inductor is used, the output capacitor has to be made large, to sustain the load during transients. Increasing the output capacitor count drives up the VR cost and footprint. The limiting (critical) values of the power-train output capacitance and the power-train inductance, which permit tight load-line regulation, have been derived in [4]–[8], respectively. A number of topological modifications to the basic interleaved buck converter have been proposed to improve the transient response, while retaining high efficiency [9]–[19].

Besides these efficiency and transient considerations, the tight load-line regulation requirements present a challenge to the controller design as well. Conventional load-line regulation (a.k.a. adaptive voltage positioning) sets the closed-loop output impedance equal to the output capacitor effective series resistance (ESR) [4], [5]. This method allows for the output capacitance to be halved for a given transient regulation window, compared to stiff output regulation. Load-line regulation implementations based on feedback current-mode control [4], [5], [8] and feedback voltage-mode control with load current injection [6], [15], have been presented, using power trains with electrolytic output capacitors. Variations of these linear control approaches are commonly adopted by industry, typically using fixed-frequency pulsewidth modulated (PWM) modulation [11]. With these techniques, the nominal system closed-loop bandwidth is tightly related to the output capacitor ESR time constant [8], [16]. With typical electrolytic capacitors having such a time constant on the order of 3–10 μs, it is straightforward for this approach to work with conventional switching frequencies in the range of 200–500 kHz. For modern VR applications, ceramic capacitors present an attractive alternative to electrolytics due to their low ESR and low effective series inductance (ESL), small footprint, and low profile. However, ceramic capacitors have ESR time constants between 20 and 200 ns, yielding the conventional load-line design framework unsuitable, since it would require a switching frequency on the order of 10 MHz [8]. Further, if ceramic capacitors with ESR matching the desired output impedance are used, their capacitance will be too low to provide adequate ripple filtering and load transient support.

The bandwidth of converters with linear feedback control is limited by stability constraints linked to the switching frequency [8], [16]. Extending the bandwidth can result in cost and board area savings, since it can reduce the required number of capacitors [17]. However, increasing the switching frequency to effect bandwidth extension results in additional switching losses. Nonlinear duty-ratio control techniques have been proposed to extend the effective bandwidth and improve transient

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A. V. Peterchev is with the Department of Psychiatry, Columbia University, New York, NY 10032 USA (e-mail: ap2394@columbia.edu).

S. R. Sanders is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720 USA (e-mail: sanders@eecs.berkeley.edu).

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[1]By convention, if the VR is embedded on the computer motherboard, it is referred to as a voltage regulator-down (VRD), while if it is mounted on a separate plug-in card, it is called a voltage regulator module (VRM).

performance [18]–[21]. However, these approaches tend to have closed-loop performance which is difficult to predict and is sensitive to noise. Hysteretic control could offer fast response as well, however it is difficult to generalize to multi-phase converters due to ripple-cancellation effects and the lack of an internal time reference for the phase shifting. Proposed multiphase hysteretic architectures [22], [23] appear to have high sensitivity to noise, as well, due to the small amplitude of the ripple signals. Finally, load-current feedforward has been used to speed up the transient response in current-mode converters with stiff voltage regulation [5], [24]. However, in [5] it is suggested that fast feedback compensation can match the performance of load-current feedforward. This may be true for particular converter designs but is not the case in general, as will be argued in this paper.

In this work, we extend the load-line regulation framework to encompass capacitor technologies with a wide range of time constants, including electrolytic and ceramic capacitors. In this context we identify the bandwidth limitations of feedback approaches. In particular, the required loop bandwidth is inversely proportional to the output capacitor size. We propose and demonstrate the use of linear load-current feedforward to extend the useful control bandwidth beyond the limits imposed by feedback stability constraints. We derive the feedforward control laws for both voltage-mode and current-mode load-line control. The load-current feedforward is used to handle the bulk of the regulation action, while the feedback is used only to compensate for imperfections of the feedforward and to ensure tight dc regulation. In this case, the size of the output capacitor is determined by large-signal transient and switching-ripple considerations, and not by the feedback stability constraint. We extend previous large-signal transient analyses to derive a critical capacitance value which accounts for the capacitor time constant, controller delay, load current slew rate, and allowable load-line overshoot. It is demonstrated that for representative ceramic-capacitor VR architectures, the large-signal and ripple constraints on the output capacitor are less restrictive than the feedback stability requirement. Therefore, eliminating the feedback stability constraint by applying load feedforward can reduce the required number of output capacitors. In particular, the electrolytic bulk capacitors in a VR design can be eliminated, and the voltage regulation can be fully supported by the ceramic high-frequency-decoupling capacitors in and around the microprocessor socket cavity, at sub-megahertz switching frequencies. The load-current estimate used in both the feedback and feedforward control laws is obtained via lossless inductor and capacitor current sensing.

In Section II, we generalize the load-line impedance to a dynamic quantity which is consistent for capacitor technologies with both large (electrolytic) and small (ceramic) ESR time constants. Section III reviews feedback load-line control methods, extends them to a generalized load-line impedance, and identifies their bandwidth limitations. Section IV introduces load-current feedforward as a means of circumventing the bandwidth limitation of pure feedback control, and derives feedforward control laws for both voltage-mode and current-mode control. Section V discusses large-signal constraints on the converter load-transient performance, and identifies a minimum (critical) capacitance value which can support the load transient. Section VI identifies requirements on the output capacitor size due to the switching ripple. Section VII compares the various constraints on the output capacitor size, in the context of microprocessor VRs, and discusses load-current estimation and PWM modulator choice. Finally, Section VIII presents simulated and experimental results on feedback and feedforward control of a four-phase buck converter with ceramic output capacitors.

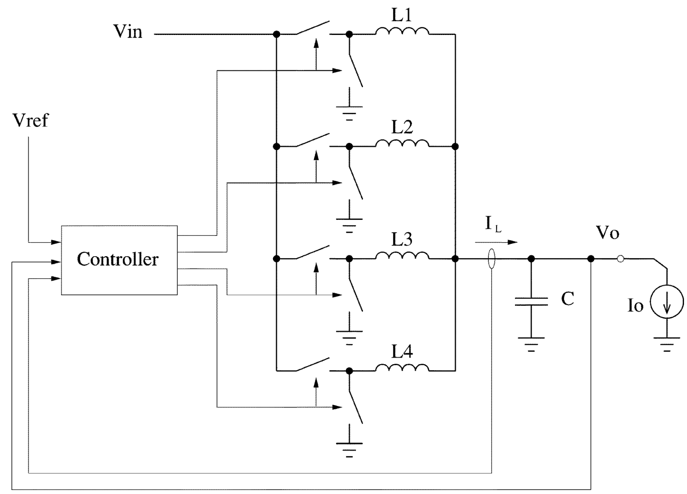

Fig. 1. Four-phase buck converter. The four phases are interleaved at 90° with respect to each other, in order to reduce the output voltage ripple and input current ripple.

II. Load-Line Impedance Regulation

Fig. 1 shows the simplified structure of a representative four-phase buck converter, commonly used in microprocessor VRs [25]. In the analysis in this paper, the multiphase converter is modelled as a single-phase converter for simplicity, unless stated otherwise. Conventional load-line control, as used in microprocessor VR applications, sets the desired closed-loop impedance R_{ref} equal to the output capacitor ESR r_C [4], [5]. While this approach works well with capacitor technologies with large ESR time constants $\tau_C = r_C C$, such as electrolytic capacitors, it is not applicable to small ESR time constant technologies, such as ceramic capacitors, due to their small capacitance per unit ESR [8], [16]. With ceramic capacitors, the capacitor size C has to be chosen large enough so that it provides adequate ripple filtering and load transient support. Due to the small ESR time constant, this results in the ESR being much less than the desired load-line impedance R_{ref}. Under these circumstances, it is natural to specify the load-line impedance dynamically, so that in the low-frequency limit the output impedance is equal to R_{ref}, and in the high-frequency limit it converges to the capacitor ESR value r_C. To achieve this, the load-line impedance can be set to

$$Z_{\mathrm{ref}} \triangleq R_{\mathrm{ref}} \frac{1 + s\tau_C}{1 + sR_{\mathrm{ref}}C}. \tag{1}$$

This is a generalization of the resistive output impedance in conventional load-line control, where $Z_{\mathrm{ref}} \triangleq R_{\mathrm{ref}}$. This approach

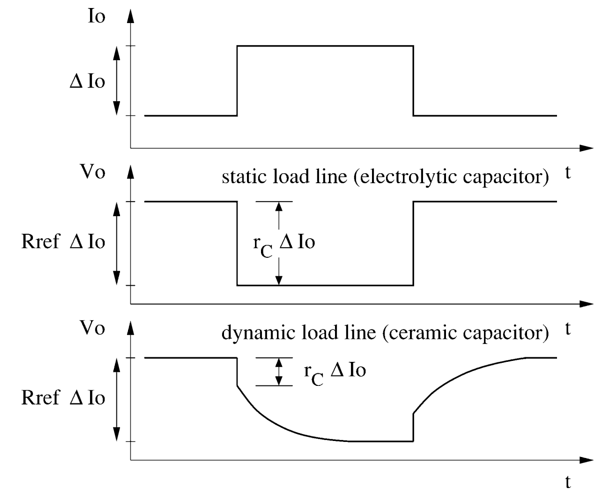

Fig. 2. Typical output voltage transient response with load-line regulation, assuming no duty-ratio saturation occurs. Illustrated are static and dynamic load-lines, which are appropriate for electrolytic and ceramic output capacitors, respectively.

reconciles the use of output capacitors with ESR lower than the specified load-line impedance. The load-line is now given by

$$V_o \rightarrow V_{\mathrm{ref}} - Z_{\mathrm{ref}} I_o. \tag{2}$$

In Fig. 2, the output voltage step response with a dynamic load-line (e.g., with a ceramic capacitor) is compared to that with a conventional static load-line (e.g., with an electrolytic capacitor). Note that this load-line impedance paradigm would be consistent with an ideal capacitor with zero ESR, where $\tau_C = 0$.

It should be noted that the controller for a ceramic-capacitor power train has to be designed so that the output impedance is regulated to Z_{ref}, and not to R_{ref}, since the latter approach will result in undesirable load-line overshoot. Consider, for example, the ΔI_o loading step in Fig. 2. Initially the output voltage will drop by $r_C \Delta I_o$ due to the capacitor ESR. If the regulator implements a static load-line with impedance $R_{\mathrm{ref}} > r_C$, the controller will try to force the output voltage to drop by $R_{\mathrm{ref}} \Delta I_o$, instead. The controller will initially decrease the duty-ratio command, instead of appropriately increasing it to handle to loading transient. Consequently, the inductor current will initially decrease, instead of increasing, eventually making the output voltage overshoot beyond the desired load-line.

III. Feedback Control Approaches and Their Limitations

Traditionally, feedback control approaches have been used to implement load-line regulation. Here we review these methods, extend them to the generalized impedance regulation described in Section II, and identify their bandwidth limitations.

A. Switching Stability Constraint

In fixed-frequency switching converters with feedback control there is a fundamental limit on the loop-gain bandwidth which results in stable closed-loop operation. In particular, feedback bandwidth which approaches or exceeds the switching frequency may result in nonlinear behaviors such as period-doubling or chaos [26]. This stability constraint can be expressed as

$$f_c < \alpha f_{\mathrm{sw}} \tag{3}$$

where f_c is the feedback unity-gain frequency, and α is a constant. According to Deslauriers *et al.* [27] the fundamental upper limit for naturally-sampled, triangle carrier PWM is $\alpha = 1/3$. For practical designs $\alpha = 1/6$ is recommended in [8]. In an interleaved N-phase buck converter the stable bandwidth can potentially be extended by N times, due to the reduced modulation delay [28]. However, in the presence of parameter mismatches among the phase legs, aliasing effects at the switching frequency may reduce the usable bandwidth [28]. Thus, (3) with $\alpha = 1/6$ stands as a practical stability guideline, with the understanding that for multi-phase designs it may be on the conservative side.

B. Load-Line Feedback

This approach is based on the principle that if an error signal formed by subtracting the desired load-line trajectory from the output voltage, is fed to a high gain feedback controller, the output voltage will track the load-line. This method was discussed in [6], and replicated in [15]. It can be used with both voltage-mode and current-mode control. Similar approaches have been used in a number of commercial integrated circuits (ICs). Some commercial ICs use the inductor current, instead of the load current, to form the load-line reference signal [11]. This results is additional derivative gain of the feedback controller which tends to improve transient performance, provided the closed-loop system is stable. In this work, we use the load current in the definition of the load-line, and relegate the control dynamics to the feedback and feedforward control laws, which provides for a clean and flexible design framework.

A small-signal block diagram of the load-line feedback scheme with a voltage-mode controller is shown in Fig. 3. Here

$$G(s) = \frac{s r_C C + 1}{s^2 LC + s(r'_L + r_C)C + 1} \tag{4}$$

is the transfer function between the controller command and the output voltage, $L = L_\phi / N$ is the total power train inductance for an N-phase converter, and r'_L is the series combination of the total inductor resistance and the average switch and input source resistance. The controller command v_c incorporates the PWM modulator voltage gain, $v_c = d \cdot V_{\mathrm{in}}$, where d is the duty ratio command and V_{in} is the input voltage. The open-loop output impedance is

$$Z_{\mathrm{oo}}(s) = \frac{r'_L (s r_C C + 1)(sL/r'_L + 1)}{s^2 LC + s(r'_L + r_C)C + 1}. \tag{5}$$

The feedback controller uses a standard PID control law, with an extra high-frequency pole $1/\tau_C$ which ideally cancels the capacitor ESR zero

$$C_{\mathrm{fb}}(s) = K \left(1 + \frac{1}{T_I s} + T_D s\right) \frac{1}{s\tau_C + 1}. \tag{6}$$

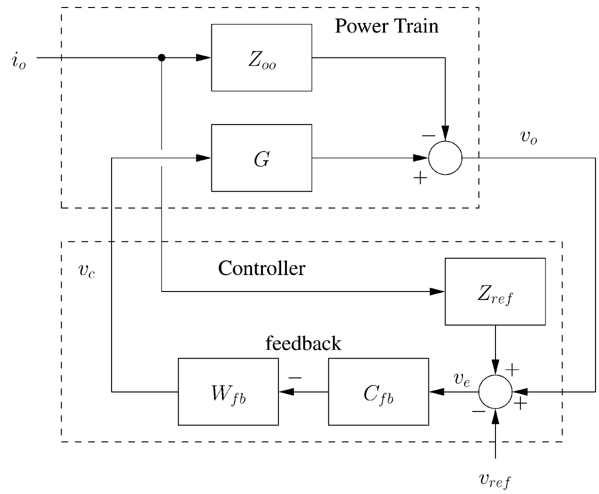

Fig. 3. Load-line feedback block diagram with voltage-mode control.

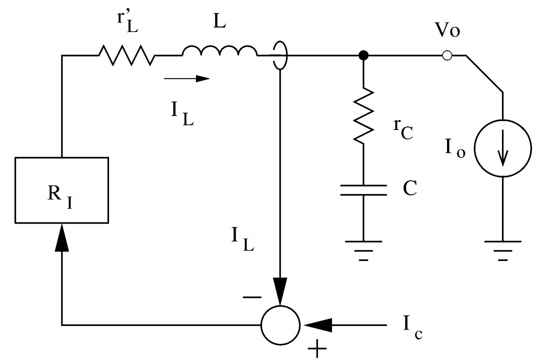

Fig. 4. Model of current modulator with current (inner) loop closed.

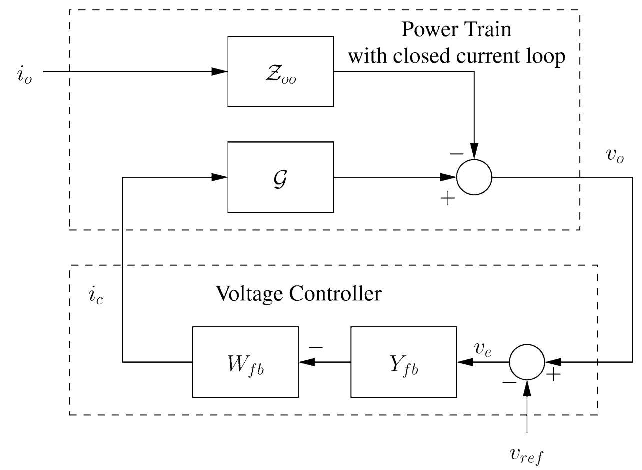

Fig. 5. Block diagram of current-mode load-line control with finite dc gain compensator Y_{fb}.

The derivative term zero and the $1/\tau_C$ pole provide a -20 dB/dec rolloff above the LC cutoff frequency, to ensure a good phase margin. Conventional design procedures can be used to choose the PID parameters to yield good phase and gain margins [29, Ch.9]. The high-frequency dynamics of the feedback loop are modelled by

$$W_{\text{fb}}(s) = e^{-st_{d,\text{fb}}} \tag{7}$$

where $t_{d,\text{fb}}$ lumps the effective delay of the modulator, the gate drivers, and the power switches.

From Fig. 3, the converter closed-loop output impedance is calculated to be

$$Z_o = Z_{\text{ref}} \frac{Z_{\text{oo}}/Z_{\text{ref}} + GW_{\text{fb}}C_{\text{fb}}}{1 + GW_{\text{fb}}C_{\text{fb}}}. \tag{8}$$

In Appendix A, it is shown that for $Z_o \rightarrow Z_{\text{ref}}$ with load-line feedback control, the loop unity gain bandwidth f_c has to be

$$f_c \gg 1/2\pi R_{\text{ref}} C. \tag{9}$$

This observation is confirmed by the simulation results in [15]. However, as discussed in Section III, to avoid closed-loop instabilities, the loop bandwidth should be below the switching frequency. Combining (3) and (9) results in a trade-off relation between the number of output capacitors required and the switching frequency used

$$C \gg \frac{1}{2\pi R_{\text{ref}} \alpha f_{\text{sw}}}. \tag{10}$$

Thus, for a given switching frequency, the output capacitor should be selected sufficiently large to meet the stability constraint.

C. Voltage Feedback With Finite dc Gain

This approach uses the fact that a power converter with finite, nonzero dc feedback gain has a finite, nonzero closed-loop output impedance. Thus, by appropriate selection of the feedback control law, the converter closed-loop output impedance can be set to a particular value. This approach is readily implementable with current-mode control, while its use with voltage-mode control is not practical [8]. This method, developed for the special case of the output impedance equal to the output capacitor ESR, was introduced in [4] and [5]. In the discussion below it is extended to the control of a general output impedance Z_{ref}, as defined in (1).

Fig. 4 gives the model of a buck converter with a current-mode controller. Parameter I_c is the current command provided by the voltage (outer) control loop, and R_I is the effective current-loop gain. The current-loop gain is modelled as

$$R_I = F_m V_{\text{in}} = \frac{V_{\text{in}}}{M_c T_{\text{sw}}} \tag{11}$$

where M_c is the compensation ramp slope, and $T_{\text{sw}} = 1/f_{\text{sw}}$ is the switching period [29, Ch.12], [30]. Without a compensation ramp ($M_c = 0$), the effective current-loop gain is infinite ($R_I \rightarrow \infty$), reflecting the sliding-mode nature of the current loop.

Fig. 5 shows a control block diagram of the complete controller. The transfer function between the current command and the output voltage, with the current-loop closed, is

$$\mathcal{G}(s) = \frac{NR_I(sr_C C + 1)}{s^2 LC + s(R_I + r'_L + r_C)C + 1} \tag{12}$$

where N is the number of phases. The corresponding open-voltage-loop output impedance is

$$\mathcal{Z}_{\rm oo}(s) = \frac{(R_I + r'_L)(sr_C C + 1)\left(s\frac{L}{R_I + r'_L} + 1\right)}{s^2 LC + s(R_I + r'_L + r_C)C + 1}. \qquad (13)$$

Note that for high current-loop gain R_I, both (12) and (13) become independent of the inductor value L, since the current loop provides for this desensitivity [29, Ch.12]. Finally, the closed-loop output impedance of the converter is

$$\mathcal{Z}_o = \frac{\mathcal{Z}_{\rm oo}}{1 + \mathcal{G}\mathcal{W}_{\rm fb}Y_{\rm fb}} \qquad (14)$$

where parameter $\mathcal{W}_{\rm fb}(s)$ models the loop delay, analogously to (7), and $Y_{\rm fb}$ is the feedback control law.

Assuming a high value of the current-loop gain ($R_I \to \infty$), ignoring the high-frequency dynamics ($\mathcal{W}_{\rm fb} = 1$), and requiring $\mathcal{Z}_o = Z_{\rm ref}$, we obtain the feedback control law

$$Y_{\rm fb} = \frac{1}{NR_{\rm ref}(1 + s\tau_C)} \qquad (15)$$

which is consistent with the derivation for the case of $R_{\rm ref} = r_C$ [4], [5]. Under this control law, the voltage-loop unity gain bandwidth is

$$f_c = \frac{1}{2\pi R_{\rm ref} C}. \qquad (16)$$

Indeed, for the case $R_{\rm ref} = r_C, f_c$ has been previously identified as a critical bandwidth which constrains the switching frequency choice [8], [16]. Analogously to Section III-B, we can combine (16) with the bandwidth stability constraint (3) to link the required output capacitance to the switching frequency

$$C = \frac{1}{2\pi R_{\rm ref}\alpha f_{\rm sw}}. \qquad (17)$$

Clearly, the voltage-loop bandwidth requirement (16) and the associated output capacitor constraint (17) are more relaxed compared to those for load-line feedback control given in (9) and (10), respectively. However, here we have assumed infinite current-loop gain. In practice, a compensation ramp may have to be introduced in the current-mode PWM modulator for stability and noise-immunity purposes, which reduces the effective current-loop gain [29, Ch.12]. If a compensation ramp is introduced, the voltage-loop control law (15) has to be modified to reflect the finite current-loop gain.

Finally, it should be pointed out that when used with peak or valley current control schemes, this method incurs a dc output voltage offset. Since the feedback loop controls the peak or valley inductor current rather than the average current in each phase, the output voltage is shifted from the reference load-line by $NR_{\rm ref}\Delta I_{L\phi,p-p}/2$, where $\Delta I_{L\phi,p-p}$ is the peak-to-peak phase current ripple. This problem can be remedied by appropriately adding a slow integrator to force the average phase inductor current to equal the current command I_c.

IV. Load-Current Feedforward Control

The load-line regulation approaches discussed in the previous sections are based on feedback, and it was shown that their bandwidth is fundamentally limited by stability constraints. Feedforward is a control paradigm which can complement feedback by providing a fast response to load-current transients. Generally, feedforward is used to cancel the effects of known disturbances, and provide anticipative action in tracking tasks [31, Ch.3], [32, Ch.7]. For example, assume that the converter load is a current source with variable current. If we can measure or estimate the variations of the load current, we can compute the appropriate control actions that would result in the desired output load-line, without invoking feedback. In this case, the load current is an exogenous variable rather than a state variable of the converter, since the load is an independent current source. Thus, the gain and bandwidth of the feedforward are not limited by stability considerations [32, Ch.7], and therefore the feedforward can provide very fast response to load changes. The major limitation of feedforward is that to calculate the feedforward control law, a model of the power train is required [31, Ch.II.3]. Since it is virtually impossible to have an exact model of the converter, feedforward cannot provide tight regulation by itself. Therefore, to effect fast and precise regulation, a combination of feedforward and feedback should be deployed: The feedforward rapidly computes the bulk of the regulation action, while the feedback damps resonances, and compensates for imperfections of the feedforward. Load-current feedforward can be used with both voltage-mode and current-mode control, and the feedforward control laws for both cases are derived below.

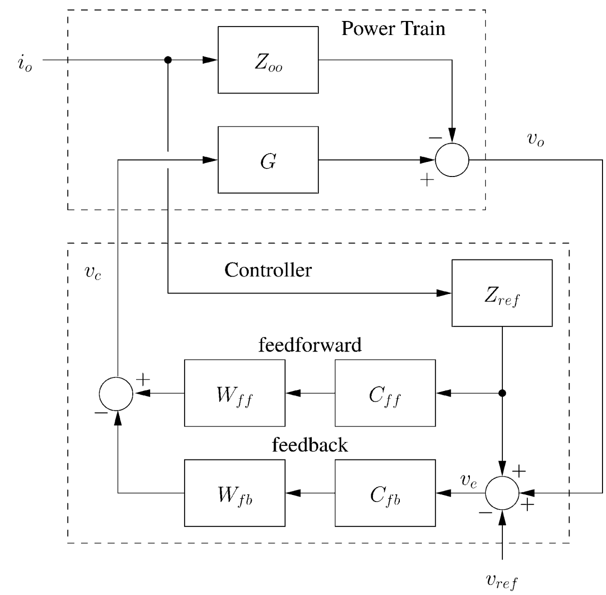

Fig. 6. Voltage-mode load-line control block diagram with load-current feedforward.

A. Voltage-Mode Control

Fig. 6 shows a block diagram of the buck converter with voltage-mode load-line control from Fig. 3 with an added load-current feedforward path. Here, $C_{\rm ff}$ is the feedforward control law, and

$$W_{\rm ff}(s) = e^{-st_d} \qquad (18)$$

models the delay of the feedforward path. The closed loop output impedance is

$$Z_o = \frac{Z_{\rm oo} + G(Z_{\rm ref}W_{\rm fb}C_{\rm fb} - W_{\rm ff}C_{\rm ff})}{1 + GW_{\rm fb}C_{\rm fb}}. \tag{19}$$

The feedforward control law can be derived by setting the closed-loop output impedance (19) equal to the desired value $Z_{\rm ref}$, yielding

$$C_{\rm ff}(s) \triangleq \frac{Z_{\rm oo} - Z_{\rm ref}}{W_{\rm ff}G}. \tag{20}$$

Note that if the ideal feedforward law (20) could be implemented, the output impedance would have the desired value $Z_o = Z_{\rm ref}$ and no feedback is necessary. In reality, this is impossible due to parameter uncertainties and the fact that $W_{\rm ff}$ contains delay, thus $C_{\rm ff}$ would be anticausal. A practical implementation $C'_{\rm ff}$ can approximate $C_{\rm ff}$ with an error $\delta C_{\rm ff}$

$$C'_{\rm ff} = C_{\rm ff} + \delta C_{\rm ff}. \tag{21}$$

Then the output impedance (19) becomes

$$Z_o = Z_{\rm ref}\left(1 - \frac{\delta C_{\rm ff}}{C_{\rm ff}} \cdot \frac{Z_{\rm oo}/Z_{\rm ref} - 1}{1 + GW_{\rm fb}C_{\rm fb}}\right). \tag{22}$$

Thus, the feedforward carries out the bulk of the regulation action, and the feedback acts only to decrease the feedforward nonideality. In particular, at low frequencies the uncertainty term in (22) approaches zero due to the high feedback gain, while at very high frequencies it is attenuated by $Z_{\rm oo}/Z_{\rm ref}$ approaching unity.

Expanding (20) yields the exact expression for the feedforward law

$$\begin{aligned} C_{\rm ff}(s) = \{&s^2 LCr_C(1 - \tau_C R_{\rm ref}/L\} \\ &+ s[L + \tau_C(r'_L - 2R_{\rm ref})] + r'_L - R_{\rm ref}\} \\ &/\{(s\tau_C + 1)(sR_{\rm ref}C + 1)W_{\rm ff}(s)\}. \end{aligned} \tag{23}$$

Noting that typically $L/R_{\rm ref} \gg \tau_C$ and $L \gg |\tau_C(r'_L - 2R_{\rm ref})|$, and further ignoring the delay term and the dc term, since dc regulation is handled by the integral feedback, the feedforward law can be approximated as

$$C_{\rm ff}(s) \approx \frac{sL}{sR_{\rm ref}C + 1}. \tag{24}$$

Thus, the design of the feedforward law with voltage-mode control requires knowledge of the power train inductance and output capacitance.

B. Current-Mode Control

The same load-current feedforward control approach can be used with current-mode control. The block diagram of the system, with the current (inner) loop closed, has the same structure as that in Fig. 6, except now the voltage-loop controller generates a current command which is fed to the current controller. The transfer function between the current command and the output voltage, with the current-loop closed, is given by (12). The open-loop output impedance is given by (13). The feedforward control law is derived analogously to that in the voltage-mode case

$$\begin{aligned} \mathcal{C}_{\rm ff}(s) = \{&s^2 LCr_C(1 - \tau_C R_{\rm ref}/L) \\ &+ s[L + \tau_C(R_I + r'_L - 2R_{\rm ref})] \\ &+ R_I + r'_L - R_{\rm ref}\} \\ &/\{NR_I(s\tau_C + 1)(sR_{\rm ref}C + 1)\mathcal{W}_{\rm ff}(s)\}. \end{aligned} \tag{25}$$

Assuming high current-loop gain ($R_I \to \infty$) and ignoring the delay term ($\mathcal{W}_{\rm ff} = 1$), the feedforward law can be approximated by

$$\mathcal{C}_{\rm ff}(s) \approx \frac{1}{sR_{\rm ref}C + 1}. \tag{26}$$

The feedback control can use a PI law

$$\mathcal{C}_{\rm fb}(s) = \frac{\mathcal{K}}{N}\left(1 + \frac{1}{\mathcal{T}_I s}\right)\frac{1}{s\tau_C + 1} \tag{27}$$

since current-mode control provides a -20 dB/dec rolloff up to the current-loop bandwidth, and hence no derivative term is necessary. The integral term may be necessary to provide infinite dc loop gain in the cases when the load has finite impedance or a compensation ramp is used, limiting the voltage loop dc gain. One major advantage of current-mode control is that, unlike the voltage-mode case, no precise knowledge of L is needed for the design of $\mathcal{C}_{\rm ff}$ and $\mathcal{C}_{\rm fb}$, thus allowing for more robust controller designs.

C. Stability With Finite-Impedance Load

The derivations above assume that the load is a variable current source with infinite impedance. However, if the load has finite impedance, the load current is a function of the output voltage,

$$I_o(V_o) = Z_{\rm load}^{-1} V_o. \tag{28}$$

This corresponds to adding a gain block $Z_{\rm load}^{-1}$ between the output voltage and the input current in the system block diagram in Fig. 6. This additional feedback loop has gain

$$\left|Z_o Z_{\rm load}^{-1}\right| \le |Z_o|\left|Z_{\rm load}^{-1}\right|. \tag{29}$$

For microprocessor designs, $|Z_o| \sim 1\ m\Omega$ and $|Z_{\rm load}| \ge 1\ \text{V}/100\ \text{A} = 10\ \text{m}\Omega$. Therefore, the loop gain magnitude in (29) is less than one. Further, Z_o and $Z_{\rm load}^{-1}$ have stable dynamics. Thus, by the small gain theorem [32, Ch.5], the closed-loop system loaded with a finite impedance is stable.

V. Large-Signal Considerations: Critical Capacitance

During large load current transients the inductor current slew rate is limited by the supply rails. The maximum voltage which can be imposed across the inductor is

$$V_L^\star = \begin{cases} V_{\rm in} - V_{\rm ref}, & \text{for loading step} \\ V_{\rm ref} - R_{\rm ref}\Delta I_o, & \text{for unloading step.} \end{cases} \tag{30}$$

Here, we are ignoring the inductor and switch resistances, which will decrease $V_L^\star$ for the loading step, and increase it for the

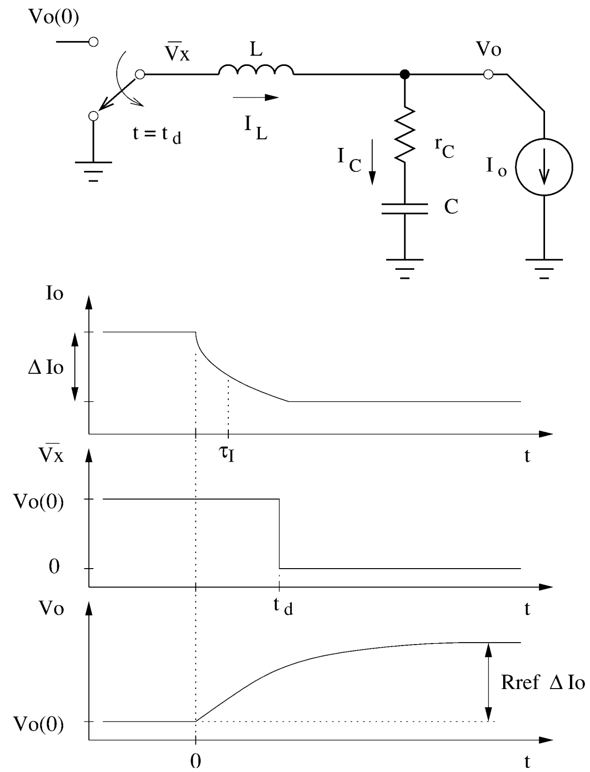

Fig. 7. Buck converter transient response model for a large unloading current step.

unloading step, by a small amount. If tight regulation is required, the output voltage should not overshoot from the specified load-line during large load transients. This requirement constrains the power filter components. In particular, for a given total (all phase inductors in parallel) inductance value, there is a minimum output capacitance value (critical capacitance) for which this requirement can be met.

The original derivation of the critical capacitance [4], [5] assumes that the load-line impedance is equal to the output capacitor ESR ($Z_{\rm ref} = r_C$). As discussed in Section II, this design choice is typical for converters using electrolytic output capacitors, however, it is not practical with ceramic output capacitors. Here we derive the critical capacitance for a more general output impedance as defined in (1) of Section II. Further, the results presented here incorporate the controller delay and the load current slew rate, which have not been previously accounted for.

Fig. 7 shows a model of the buck converter response for a large unloading transient. The unloading current step can be modelled by a magnitude ΔI_o and a time constant τ_I which characterizes the rise/fall time (or slew rate). The controller is assumed to have a response delay t_d, after which it applies maximum control effort by saturating the duty ratio to zero. Linear-system time constants associated with the controller response can be incorporated in t_d. Further, the switching node voltage is modelled as an average value over one switching period $\bar{V}_x$, since the delay effects of the switching action can also be lumped in t_d. Finally, current microprocessor VR specifications allow the output voltage to overshoot by some amount $\Delta V_{\rm os}$ above the defined load-line during unloading transients (see Table I), to reduce the output capacitor requirement [3]. The loading transient can be analyzed analogously. For this model, the critical capacitance required for tight transient load-line support is derived in Appendix B, yielding (31), shown at the bottom of the page, where $t_L = L\Delta I_o/V_L^\star$ and $L_{\rm crit} = \tau_C V_L^\star/\Delta I_o$. The above expression yields two values for the critical capacitance—one for the loading, and one for the unloading transient—which typically have different $V_L^\star$, as shown in (30). The larger value of the two should be used in design. The quantity $L_{\rm crit}$ has been identified as a critical inductance value below which the output voltage transient is independent of the inductance value [6]–[8]. In [6]–[8], it is suggested that the converter total inductance should be designed to match this critical inductance value. This is readily implementable in designs using electrolytic capacitors, which have a large ESR time constant. However, it is clear that for capacitor technologies with a small ESR time constant, such as ceramic capacitors, this design choice implies impractically small inductance values. The result in (31) presents a consistent framework for transient design with inductances above the critical value. They indicate that for designs with a small capacitor ESR time constant, where typically $L > L_{\rm crit}$, reducing the inductance value is beneficial, from a transient performance perspective, since this decreases the required output capacitance via parameter t_L. These results also show how the converter delay and the load current slew rate affect the capacitance choice: larger controller delay and load slew rate require larger output capacitance to handle the transient.

VI. Switching-Ripple Considerations

The switching-ripple constrains the power train design with regard to both regulation performance and efficiency. The inductor current ripple of a single phase has a peak-to-peak amplitude of

$$\Delta I_{L\phi,p-p} = \frac{V_{\rm in} T D(1-D)}{L_\phi} \tag{32}$$

and a frequency of $f_{\rm sw}$ [29, Ch.2]. The inductor current ripple incurs conductive and core losses which may aggravate the conversion efficiency, and limit high-frequency performance [29, Ch.13]. The total inductor current (sum of all inductor currents) ripple of an N-phase interleaved buck converter can be shown to be

$$\Delta I_{L,p-p} = \frac{V_{\rm in} T D^*(1-ND^*)}{L_\phi} \tag{33}$$

$$C_{\rm crit} \approx \begin{cases} (\tau_C + t_d - \tau_I)/(R_{\rm ref} + \Delta V_{\rm os}/\Delta I_o), & \text{for } L \le L_{\rm crit}, \\ \left(\frac{t_L}{2} + \frac{\tau_C^2}{2t_L} + t_d - \tau_I\right)\Big/(R_{\rm ref} + \Delta V_{\rm os}/\Delta I_o), & \text{for } L > L_{\rm crit}, \end{cases} \tag{31}$$

where $D^* = \mathrm{mod}(D, 1/\mathrm{N})$. The total inductor current ripple frequency is Nf_{sw}. In buck converters with a coupled inductor, the total inductor current ripple is also given by (33), however the phase current ripple is smaller than that in conventional uncoupled implementations [9], [10]. In particular, the phase current ripple is equal to the total-inductor current ripple (33) divided by the number of phases N

$$\Delta I_{L\phi,p-p,\mathrm{coupled}} = \frac{V_{\mathrm{in}} T D^*(1/N - D^*)}{L_\phi} \qquad (34)$$

which is always smaller than (32) for a given set of power-train parameters.

The total inductor current ripple (33) results in voltage ripple across the output capacitor and its ESR. The output voltage ripple can be accurately approximated by combining the magnitudes of the capacitor and ESR ripples, yielding

$$\Delta V_{o,p-p} \approx \frac{\Delta I_{L,p-p}}{C}\sqrt{\left(\frac{T}{8N}\right)^2 + \tau_C^2}. \qquad (35)$$

Note that expression (35) does not include the ripple contribution due to the output capacitor effective series inductance (ESL). The ESL depends strongly on the capacitor packaging and circuit layout [33], [34]. Since the output voltage ripple affects the regulation performance, it can be yet another factor constraining the choice of output capacitor. Finally, note that while the interleaved multiphase operation reduces the output voltage ripple (35), it does not affect the inductor current ripple in the individual phases (32), in a conventional, uncoupled inductor design.

VII. Application to Microprocessor VRs

Load-line regulation is adopted as a standard control method in microprocessor VRs [3]. Hence, the discussion above can be applied directly to the design of VRs.

A. Output Capacitor Size

Three important design considerations that impose a lower limit on the VR's output capacitance were discussed in the previous sections: First, the capacitor size is constrained by feedback stability requirements as given by (10) and (17). Second, the critical capacitance requirement (31) has to be met for both the loading and unloading transients. Third, the output voltage ripple (35) limits the capacitor choice as well. In Fig. 8, these constraints are plotted versus switching frequency for a number of VR architectures, assuming VR parameters from Table I, and $N = 4, \tau_C = 24$ ns, $\Delta I_{L\phi,p-p} = 8$ A, $\Delta V_{o,p-p} = 16$ mV, $t_d = 100$ ns, and $\alpha = 1/6$. For these specifications, the phase inductance is calculated from (32) for the VR examples with uncoupled inductors, and from (34) for the coupled-inductor design. Fig. 8(a) characterizes a conventional 12 V-input VR topology. Fig. 8(b) presents a coupled-inductor implementation [9], [10] which meets the specified phase current ripple requirement with much smaller total inductance (see Section VI). As a result of the lower total inductance, the loading and unloading transient constraints on the output capacitance are relaxed, compared to the uncoupled case. However, the lower inductance also yields higher total inductor current ripple, requiring larger capacitance to maintain the specified output voltage ripple. Fig. 8(c) depicts a converter with "body braking" which turns off the synchronous rectifier when the duty-ratio command saturates to zero, forcing con-

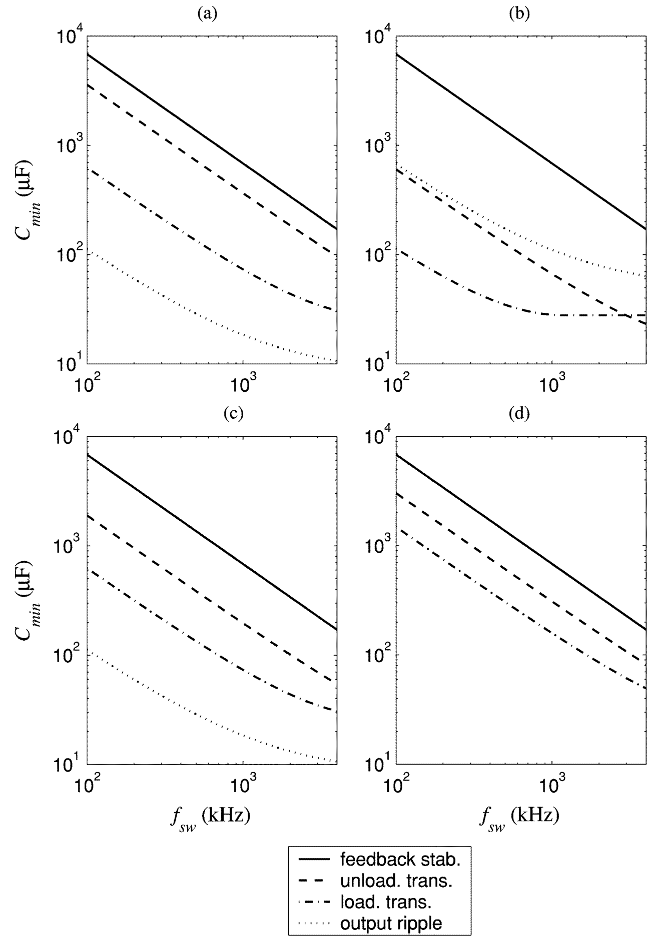

Fig. 8. Minimum output capacitance constraints versus switching frequency, associated with unloading and loading transient response, feedback stability, and output ripple. (a) $V_{\mathrm{in}} = 12$ V. (b) Coupled inductors. (c) Synchronous rectifier turned off during unloading. (d) $V_{\mathrm{in}} = 5$ V. Note: In (d), the output ripple constraint yields $C_{\min} < 10\ \mu$F which is below the range of the plot.

TABLE I
Sample Microprocessor VR Specifications

V_{in}	input voltage	12 V
V_{ref}	reference output voltage	1.2 V
$I_{o,max}$	max. load current	78 A
ΔI_o	max. dynamic load step	55 A
τ_I	load step time constant	85 ns
R_{ref}	closed-loop output impedance	1.4 mΩ
ΔV_o	output tolerance band	± 25 mV
ΔV_{os}	max. extra unloading overshoot	50 mV
Δt_{os}	max. extra overshoot duration	25 μs

Source: Intel Corp. [3]

duction through the body diode, and thus increasing the voltage across the inductor by a diode drop V_D [11]. In this calculation, it is assumed that $V_D = 1$ V. Fig. 8(d) characterizes the second stage in a two-stage VR topology, powered from an intermediate 5-V bus [12]. Note that in all cases the feedback stability requirement dominates the other constraints. This is especially true for architectures that are specifically tailored for efficient low-conversion-ratio operation [Fig. 8(b)–(d)]. Importantly, if load-current feedforward is used, as discussed in Section IV, the feedback stability constraint is removed since ideally there are no stability limitations of the feedforward control path. In such a case, Fig. 8 suggests that the size of the output capacitor can be reduced by factors of at least 2 to 8, depending on the architecture used. Thus, the regulation specification can be met with a small number of multilayer ceramic capacitors (MLCCs) in the range of hundreds of μF at sub-MHz switching frequencies.

B. Load-Current Estimation

The load feedforward control strategy discussed in Section IV assumes that the load current is measured. Sensing the load current directly is not practical since it will require inserting a sense resistor in the load current path, thus increasing the output impedance and power loss, or using an expensive Hall-effect current sensor. Alternatively, the load current can be reconstructed from estimates of the inductor and capacitor currents since [1], [6], [15]

$$I_o = I_L - I_C. \tag{36}$$

The inductor current can be estimated with an RC filter connected in parallel with the inductor, and having time constant equal to this of the inductor. This "lossless inductor sensing" approach has been used successfully in commercial products [11]. The capacitor current can be estimated in the same way. A VR implementation diagram, using this load current estimation approach and passively summing the inductor current estimates of the different phases [1], [15] is shown in Fig. 9.

In the case of perfect matching of the estimator and power train parameters, the injection of the load current estimate in the controller does not affect the closed-loop poles and zeros of the system. This is due to the fact that I_L and I_C contain the same state information, when the load is a current source, and this state information is subtracted out when the two are combined in (36) yielding the exogenous variable I_o. In practice, there typically is some mismatch between the estimator and power train parameters, resulting in the load current estimate becoming a function of the converter state variables and hence altering the system pole and zero locations. For small mismatches this effect is small, and can be tolerated in a properly designed controller.

Finally, other load current estimation approaches can be deployed as well. For example, methods involving adaptive parameter estimation may provide a more accurate and robust load-current estimate.

C. PWM Modulator

A switch modulation scheme having a very low latency is essential for achieving a fast controller response with load-current feedforward. Good candidates include unlatched level-sensitive PWM (with some hysteresis for noise immunity), leading-edge latched PWM, two-sided latched PWM [35], and valley current-mode control [36]. All of these have turn-off latency equal to or less than the steady-state on-pulse-width, which is about a tenth of the switching period in 12 V-input VRs.

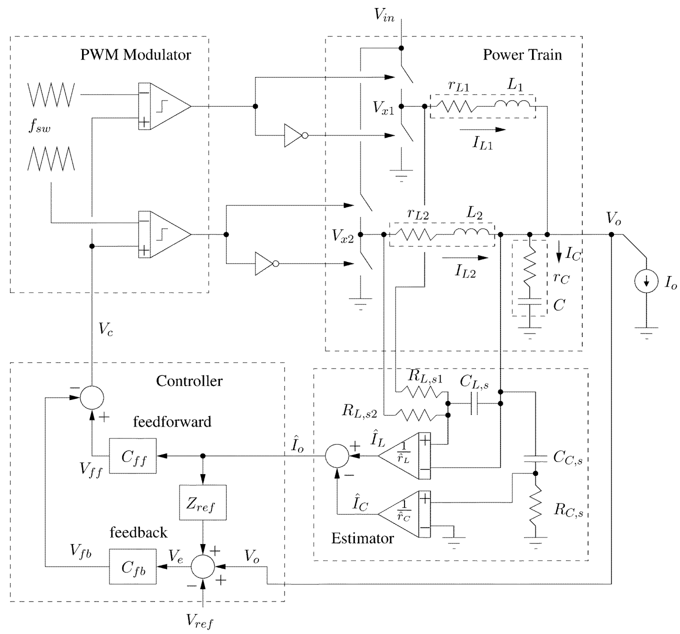

Fig. 9. Implementation diagram of a two-phase buck converter with load-line regulation and estimated load-current feedforward.

D. Dynamic Reference Voltage

In this discussion we have assumed that V_{ref} is constant. In modern microprocessor systems V_{ref} can be adjusted during operation. However, this happens at slow rates compared to changes in the load current (e.g., reference voltage slew rate of 2.2 mV/μs, [3]), and hence tracking it does not present a substantial challenge. In fact, a simple and effective reference voltage feedforward, providing good tracking up to the LC cutoff frequency, can be accomplished by directly adding V_{ref} to the input of the PWM modulator.

VIII. Simulations and Experimental Results

A. Converter Implementation

To demonstrate the use of load-current feedforward to improve load-line regulation performance, a four-phase version of the controller structure in Fig. 9 was implemented. A synchronous buck converter board (International Rectifier IRDCiP2002-C) was modified to incorporate estimated load-current feedforward. The on-board PWM modulator (Intersil ISL6558) uses voltage-mode, latched trailing-edge modulation with phase-current balancing. The converter parameters are summarized in Table II. The feedforward law (24) from Section IV-A was used.

B. Simulations

The system was simulated in PSIM (Powersim Inc.). Figs. 10 and 11 show the converter transient response to load steps of different magnitude, with and without load-current feedforward. In Fig. 10, a small 8-A load step is depicted. With load-current

TABLE II
EXPERIMENTAL CONVERTER PARAMETERS

Power Train		
N	number of phases	4
V_{in}	input voltage	12 V
$I_{o,max}$	max. load current	120 A
$r_{h\phi}$	high-side switch on-resistance	21 mΩ
$r_{l\phi}$	low-side switch on-resistance	3 mΩ
L_ϕ	phase inductors	390 nH @ 15 A
$r_{L\phi}$	inductor ESR & trace resistance	0.7 mΩ
C_{bulk}	output bulk cap.	8×100 μF (ceram.)
τ_{Cbulk}	output bulk cap. ESR time const.	0.2 μs
C_{hf}	output high-freq. decoupling cap.	10 + 0.1 μF (ceram.)
τ_{Chf}	output high-freq. cap. ESR time const.	24 ns
PID Controller		
V_{ref}	reference voltage	1.3 V
R_{ref}	closed-loop output impedance	1.3 mΩ
f_{sw}	switching frequency	1 MHz
K	proportional gain	20
T_I	integral time	17 μs
T_D	derivative time	3.7 μs
	1^{st} high-freq. pole	0.55 MHz
	2^{nd} high-freq. pole	1.5 MHz
t_d	control delay before modulator	100 ns
Loop Gain		
PM	phase margin	47°
GM	gain margin	10 dB
f_c	unity gain frequency	200 kHz
Load-Current Estimator		
$R_{L,s\phi}$	I_L estimator res. per phase	30.9 kΩ
$C_{L,s}$	I_L estimator cap.	66 nF
$R_{C,s}$	I_C estimator res.	222 Ω
$C_{C,s}$	I_C estimator cap.	560 pF

feedforward the output voltage adheres tightly to the prescribed load-line [Fig. 10(a)]. In Fig. 10(b), it can be seen that the feedforward path contributes the bulk of the duty-ratio command signal, while the feedback signal has a small magnitude. In contrast, without load-current feedforward, the control effort is determined solely by the feedback path, and the output voltage deviates substantially from the desired load-line. The feedback unity-gain bandwidth is limited to 200 kHz, which is one-fifth of the switching frequency, for the stability reasons discussed in Section III-B. However, according to (9), for the load-line feedback approach to work successfully, the bandwidth has to be substantially larger than $1/2\pi R_{\mathrm{ref}}C = 153$ kHz, which could not be achieved here due to the stability constraint. Clearly, the load-current feedforward circumvents this limitation by producing a large, fast, exogenous control signal.

Fig. 11 depicts the converter response to a large 52-A load current transient. The loading transient is a scaled version of the 8-A loading response, since the system has linear average behavior. The unloading step, however, results in duty-ratio saturation at zero, due to the low output voltage. The converter behavior under duty-ratio saturation is consistent with the discussion in Section V. Indeed, solving (31) for the unloading voltage overshoot yields $\Delta V_{\mathrm{os}} = 67$ mV which matches the simulation. Notice that, compared to pure feedback control, the load-current feedforward decreases the output voltage overshoot, since it drives the duty ratio to saturation faster.

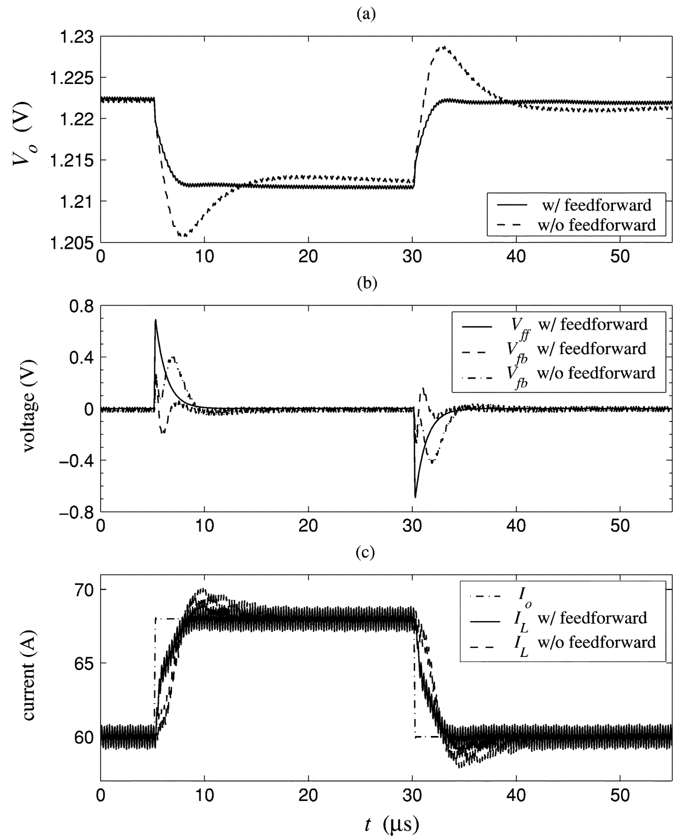

Fig. 10. Simulated 8-A load transient, from 60 A to 68 A to 60 A, with and without load-current feedforward. (a) Output voltage. (b) Duty ration command (ac component). (c) Load and total inductor current.

C. Hardware Measurements

Fig. 12 shows the experimental prototype transient response, with and without estimated load-current feedforward, for 52-A loading and unloading transients, analogously to Fig. 11. Due to hardware constraints of the pulsed load circuit, the loading current step has a time constant of about 250 ns. The unloading current step is much faster, completing the step in less than 200 ns.

From the figures it can be seen that the estimated load current follows very well the measured current with a delay of about 100 ns. The 4-MHz switching noise present in the load-current estimate results from parasitic coupling to the sense wires which were soldered on top of the converter board. The switching noise does not affect the dc regulation precision because it is attenuated by the PID controller. Further, in a dedicated implementation, the sensing can be done through buried, shielded PCB traces, thus reducing both electrostatic and magnetic pickup.

The loading transient in Fig. 12(a) resembles closely the simulation in Fig. 11. With pure feedback control the output voltage sags by 35 mV below the load-line, corresponding to overshoot of more than 50%. On the other hand, load-current feedforward effects tight load-line regulation. The unloading transient in Fig. 12(b) is similar to the one in Fig. 11 as well. The combined feedback and feedforward control produces a slightly better voltage response than the feedback alone, implying a faster transition to duty-ratio saturation. The improvement with feedforward control is not as substantial as that for the loading transient, since the duty-ratio saturation fundamentally limits the performance. An overshoot of about 85 mV is observed,

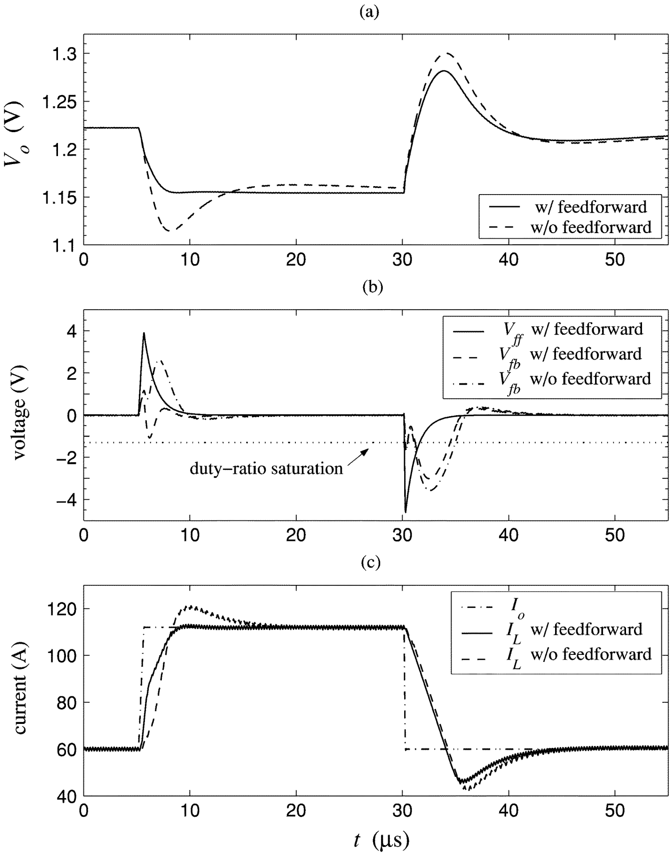

Fig. 11. Simulated 52-A load transient, from 60 A to 112 A to 60 A, with and without load-current feedforward. (a) Output voltage. (b) Duty ration command (ac component). (c) Load and total inductor current.

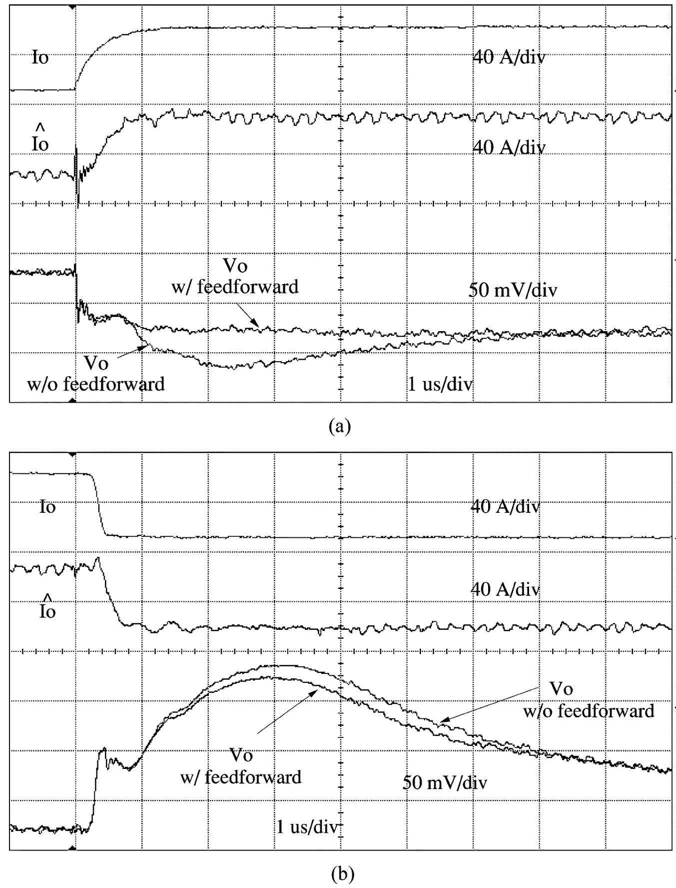

Fig. 12. Experimental 52-A load transient, with corresponding estimated load current, with and without load-current feedforward. (a) Loading step from 60 to 112 A. (b) Unloading step from 112 to 60 A.

which is expected since the duty ratio saturates to zero about 300 ns after the beginning of the step, and (31) predicts overshoot of $\Delta V_{\mathrm{os}} = 80$ mV for these conditions. The transient regulation here can be enhanced if the synchronous rectifier is turned off (body braking), or if a smaller total inductance is used (e.g., with coupled-inductors), as discussed in Section VII-A. Finally, Fig. 13 shows a smaller, 8-A experimental unloading transient which parallels the simulation in Fig. 10 with some additional sensing and measurement noise associated with the prototype. Again, it is clear that the combination of feedback and feedforward provides tighter output impedance regulation than feedback alone.

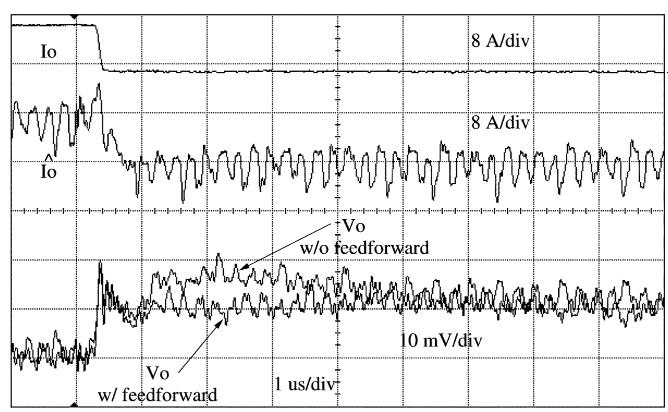

Fig. 13. Experimental 8-A unloading transient, from 68 A to 60 A, with corresponding estimated load current, with and without load-current feedforward.

IX. Conclusion

This paper presented a consistent framework for load-line regulation of the buck converter using output capacitors with an arbitrary ESR time constant, encompassing electrolytic and ceramic technologies. In both current-mode and voltage-mode control, load-current feedforward can extend the useful bandwidth beyond that achievable with pure feedback, since feedforward is not limited by stability constraints. The load-current feedforward is used to handle the bulk of the regulation action by providing a fast duty-ratio control signal. The feedback is used to compensate for imperfections of the feedforward and to ensure tight dc regulation. With load-current feedforward, the output capacitor size is limited only by large-signal transient and switching-ripple considerations. In particular, for representative ceramic-capacitor VR architectures, the large-signal and ripple constraints are shown to be less restrictive than the stability requirement, indicating that the use of load-current feedforward is advantageous in this application. The load current can be estimated from the inductor and capacitor voltages with simple RC networks, or with another lossless sensing method. Different types of PWM modulators can be used as long as they have low latency. The ability of estimated load-current feedforward to provide tighter load-line regulation than pure feedback control was demonstrated with an experimental 12-to-1.3 V, all-ceramic capacitor, multi-phase buck converter. These results point to the feasibility of microprocessor VR implementations using only a small number of ceramic output capacitors.

APPENDIX

A. Bandwidth Requirement for Load-Line Feedback Control

Load-line feedback control was discussed in Section III-B. Here, we derive a feedback-loop bandwidth requirement which guarantees the desired output-impedance regulation with this type of control. Assume a perfectly designed PID controller which provides a -20 dB/dec rolloff of the loop gain $C_{\text{fb}}W_{\text{fb}}G$ with a unity gain bandwidth of $\omega_c = 2\pi f_c$

$$C_{\text{fb}}(s)W_{\text{fb}}(s)G(s) = \omega_c/s. \tag{37}$$

The closed-loop output impedance (8) then becomes

$$Z_o = Z_{\text{ref}}\frac{Z_{\text{oo}}/Z_{\text{ref}} + \omega_c/s}{1+\omega_c/s}. \tag{38}$$

At low frequencies, $s \rightarrow 0$ and $Z_o \rightarrow Z_{\text{ref}}$, as desired. At high frequencies, the open-loop impedance is dominated by the output capacitor

$$Z_{\text{oo}} \approx \frac{1+s\tau_C}{sC}, \quad \text{for } |s| > \frac{1}{\sqrt{LC}} \tag{39}$$

where τ_C is the capacitor ESR time constant. Substituting (39) in (38), expanding Z_{ref} to its definition in (1), and rearranging terms, we obtain

$$Z_o \approx Z_{\text{ref}} \cdot \frac{\frac{1}{\omega_c R_{\text{ref}} C} + 1 + \frac{s}{\omega_c}}{1+\frac{s}{\omega_c}}. \tag{40}$$

Clearly, if $Z_o \rightarrow Z_{\text{ref}}$, then it must be true that $\omega_c \gg 1/R_{\text{ref}}C$, or, equivalently, $f_c \gg 1/2\pi R_{\text{ref}}C$.

B. Critical Capacitance Calculation

Fig. 7 shows a model of the VR response for a large unloading transient. The unloading current step can be modeled by a magnitude ΔI_o and a time constant τ_I which characterizes the slew rate

$$I_o(t) = I_o(0) - \Delta I_o(1-e^{-t/\tau_I}) \tag{41}$$

for $t \geq 0$.

Following the load step at $t = 0$, the controller reacts after some delay t_d inherent in a physical implementation (Fig. 7). Before the controller has reacted, for $0 \leq t < t_d$, the inductor current remains approximately at its initial value $I_L \approx I_o(0)$, since the output voltage practically stays constant. Then, the capacitor current is

$$I_C(t) = I_L - I_o(t) \tag{42}$$

and the capacitor voltage is

$$V_C(t) = \frac{1}{C}\int_0^t I_C(t')dt' + V_o(0) \tag{43}$$

where

$$V_o(0) = V_{\text{ref}} - R_{\text{ref}}I_o(0). \tag{44}$$

The output voltage is then

$$\begin{aligned} V_o(t) &= V_C(t) + r_C I_C(t) \\ &= \frac{\Delta I_o}{C}\left[t + (\tau_C - \tau_I)\left(1-e^{-t/\tau_I}\right)\right] + V_o(0) \end{aligned} \tag{45}$$

for $0 \leq t < t_d$.

After the delay, the maximum control effort the controller can exert is to saturate the duty ratio to zero. Thus, for $t \geq t_d$, the inductor voltage is

$$\begin{aligned} V_L(t) &= -V_o(t) \\ &\approx -V_{\text{ref}} + R_{\text{ref}}I_o(t) \\ &\approx -V_{\text{ref}} + R_{\text{ref}}(I_o(0) - \Delta I_o) \\ &\triangleq -V_L^\star \end{aligned} \tag{46}$$

ignoring the load current time constant ($\tau_I = 0$). These approximations are reasonable, since under duty ratio saturation $V_L(t)$ is dominated be the constant V_{ref}. The inductor current is then

$$I_L(t) = \Delta I_o - V_L^\star(t-t_d)/L. \tag{47}$$

Thus, the output voltage is

$$\begin{aligned} V_o(t) = \frac{\Delta I_o}{C}\Big[t &- \frac{1}{2t_L}(t-t_d)^2 - \frac{\tau_C}{t_L}(t-t_d) \\ &+ (\tau_C - \tau_I)\left(1-e^{-t/\tau_I}\right)\Big] + V_o(0) \end{aligned} \tag{48}$$

for $t \geq t_d$, where $t_L = L\Delta I_o/V_L^\star$.

We require that the output voltage does not exceed the load-line specification

$$V_o(t) \leq V_o(0) + R_{\text{ref}}\Delta I_o. \tag{49}$$

Since the maximum voltage value $\max(V_o)$ is reached at time $t_{\max} \geq t_d$, the critical capacitance can be derived from (48), by setting

$$\max(V_o) \triangleq V_o(0) + R_{\text{ref}}\Delta I_o. \tag{50}$$

The time $t_{\max}$ when the maximum voltage value is reached, can be obtained by setting the first derivative of (48) to zero, and solving for t

$$\begin{aligned} \frac{dV_o(t)}{dt} = \frac{\Delta I_o}{C}\Big[1 &- \frac{1}{t_L}(t - t_d + \tau_C) \\ &+ \left(\frac{\tau_C}{\tau_I} - 1\right)e^{-t/\tau_I}\Big] \triangleq 0. \end{aligned} \tag{51}$$

The above equation is transcendental, and thus an analytical solution for t cannot be derived in general. However, for the case of high slew rate load steps (small τ_I), which are most challenging in practice, the exponential term in (51) has negligible contribution to the solution $t_{\max}$, and can therefore be ignored. Further, the maximum voltage cannot physically occur before time t_d, thus

$$t_{\max} \approx \begin{cases} t_d, & \text{for } L \leq L_{\text{crit}} \\ t_d + t_L - \tau_C, & \text{for } L > L_{\text{crit}} \end{cases} \tag{52}$$

where $L_{\text{crit}} = \tau_C V_L^{\star}/\Delta I_o$. In the general case, $t_{\max}$ can be obtained by solving (51) numerically.

Combining (48) and (51) to eliminate the exponential term, and substituting $t_{\max}$ for t, we obtain an expression for $\max(V_o)$. Inserting the result in (50) and solving for C we obtain

$$C_{\text{crit}} = \frac{1}{R_{\text{ref}}}\left[t_{\max} + \tau_C - \frac{(t_{\max} - t_d)^2}{2t_L} - \frac{(\tau_C + \tau_I)(t_{\max} - t_d) + \tau_C \tau_I}{t_L}\right]. \tag{53}$$

Substituting the approximate value of $t_{\max}$ from (52) in the above expression yields

$$C_{\text{crit}} \approx \begin{cases} (\tau_C + t_d - \tau_I)/R_{\text{ref}}, & \text{for } L \leq L_{\text{crit}} \\ \left(\frac{t_L}{2} + \frac{\tau_C^2}{2t_L} + t_d - \tau_I\right)\Big/ R_{\text{ref}}, & \text{for } L > L_{\text{crit}}. \end{cases} \tag{54}$$

This derivation assumes that the inductor current ripple is small compared to the full load step. A discussion of the effect of large inductor current ripple on transient performance can be found in [37].

Finally, if the output voltage is allowed to overshoot above the defined load-line during large transients, this overshoot ΔV_{os} can be added on the right-hand side in (49) and (50). This results in a modified critical capacitance value (31) which is less stringent than (54) for $\Delta V_{\text{os}} > 0$.

Acknowledgment

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Angel V. Peterchev (S'96–M'05) received the A.B. degree in physics and engineering sciences from Harvard University, Cambridge, MA, in 1999, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 2002 and 2005, respectively.

He is presently a Postdoctoral Research Scientist with the Department of Psychiatry, Columbia University, New York, where he works on transcranial magnetic brain stimulation. In the Summer of 2003, he was a Co-op at the Portable Power Systems Group, National Semiconductor Corporation, Santa Clara, CA. From 1997 to 1999, he was a Member of the Rowland Institute at Harvard, where he developed scientific instrumentation. From 1996 to 1998, he was a Student Researcher with the Harvard-Smithsonian Center for Astrophysics. His research interests are in mechanisms, technology, and application paradigms of electromagnetic brain stimulation, pulsed power circuits, and analog and digital control of power converters.

Dr. Peterchev received the 1999 Tau Beta Pi Prize from Harvard University and a 2001 Outstanding Student Designer Award from Analog Devices, Inc.

Seth R. Sanders (M'88) received the S.B. degrees in electrical engineering and physics and the S.M. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, 1985, and 1989, respectively.

He was a Design Engineer with Honeywell Test Instruments Division, Denver, CO. Since 1989, he has been on the faculty of the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is presently a Professor. During the 1992–1993 academic year, he was on industrial leave with National Semiconductor, Santa Clara, CA. His research interests are in high frequency power conversion circuits and components, in design and control of electric machine systems, and in nonlinear circuit and system theory as related to the power electronics field. He is presently actively supervising research projects in the areas of renewable energy, novel electric machine design, and digital pulse-width modulation strategies and associated IC designs for power conversion applications.

Dr. Sanders received the NSF Young Investigator Award in 1993 and multiple Best Paper Awards from the IEEE Power Electronics and IEEE Industry Applications Societies. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-At-Large of the IEEE PELS Adcom.