Analytical and Practical Analysis of Switched-Capacitor DC-DC Converters

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Abstract

Switched-capacitor DC-DC converters are useful alternatives to inductor-based converters in many low-power and medium-power applications. This work develops a straightforward analysis method to determine a switched-capacitor converter's output impedance (a measure of performance and power loss). This resistive impedance is a function of frequency and has two asymptotic limits, one corresponding to very high switching frequency where resistive paths dominate the impedance, and one corresponding to very low switching frequency where charge transfers among idealized capacitors dominate the impedance. An optimization method is developed to improve the performance of these converters through component sizing based on practical constraints. Several switched-capacitor converter topologies are compared in the two asymptotic limits. Switched-capacitor converter performance (based on conduction loss) is compared with that of two magnetics-based DC-DC converters. At moderate to high conversion ratios, the switched-capacitor converter has significantly less conduction loss than an inductor-based buck converter. Some aspects of converter implementation are discussed, including the power loss due to device parasitics and methods for transistor control. Implementation using both integrated and discrete devices is discussed. With the correct analysis methods, switched-capacitor DC-DC converters can provide an attractive alternative to conventional power converters.

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1 Introduction and Motivation

Switched-capacitor power converters are often used to provide simple power-conversion functions at low power levels. These functions include doubling, halving and inverting the input voltage, and can be combined to achieve other conversion ratios. Typical applications include RS232 level converters and FLASH memory programming voltage generators. These standard converters are often unregulated or supplemented with a linear regulator for voltage regulation.

However, analysis methods for switched-capacitor (SC) converters are not well-developed and often involve complicated network-based formulations. This work develops a simple method to determine the primary performance metric of a SC converter: the output impedance. The output impedance is a real quantity that determines the voltage drop or sag on the output terminal based on the load current. The power loss in the circuit, due to capacitor charging and switch conduction losses, is also equal to the power dissipated in the output impedance if modeled as a physical resistance. The single output impedance parameter represents both the efficiency and output regulation of a SC converter.

The simple formulation developed in this work permits optimization of the capacitor sizes to meet a constraint such as a total capacitance or total energy storage limit, and also permits optimization of the switch sizes subject to constraints on total switch conductances or total switch volt-ampere (V-A) products. These optimizations are carried out for a set of representative switched-capacitor topologies. These optimizations then permit comparison among the switched-capacitor topologies, and comparisons of SC converters with conventional magnetic-based dc-dc converter circuits, in the context of various application settings.

Implementations of SC converters involve a number of other considerations. First, the power switches used must be controlled. Level-shifting circuitry is often used to translate the clock to drive each switch at the correct voltage level. Additionally, the power required to drive the switches (the gating loss) is considered. Each capacitor and switch also has parasitic elements: stray capacitance to ground or resistance in the conduction path. The loss from these components is considered and used to set further limits on the performance of SC converters. Finally, the output impedance analysis and parasitic effects is verified through several device-level simulations.

The comprehensive analysis and design calculations given here are new, but connect with the analysis framework developed in the pioneering work of reference [4]. The work in [4, 10] offered a network theoretic formulation for computation of open-circuit dc-dc conversion ratios, and a rather involved method for computation of output impedance. Reference [4] and other previous analysis work [2, 3] mainly focused on the performance analysis (i.e. output impedance computation) for a single converter, in each case.

2 A Simple Model Simplification for Single-Output Converters

Previous analysis methods [4, 10] use the fundamental loop matrices and the fundamental cut-set matrices to derive a converter's output impedance. Those methods require a strong understanding of circuit theory and require that a number of matrix equations be solved. This analysis is complex and difficult to understand from an intuitive standpoint. For single-output converters, a simpler method is developed in this work to find the output impedance.

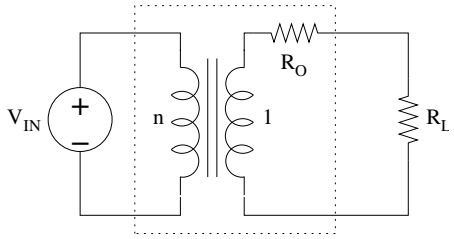


Figure 1: Model of switched-capacitor converter

Under the single assumption that there are no charge leakage paths, due to continuous leakage current or parasitic switched capacitances, the steady-state performance of a switched-capacitor power converter can be related to its output impedance, as captured in the model of Figure 1. With this model, the converter provides an ideal dc voltage conversion ratio under no load conditions, and all losses are manifested by voltage drop associated with non-zero load current. Note that losses associated with driving switches are neglected for the present but will be considered in section 4.3. Further, with the model in figure 1, the charge transfer (in steady state) between the input and output is fixed by the ratio n, a rational number [4]. The resistive impedance accounts for the losses due to capacitor switching and resistive conduction losses.

The initial analysis will consider circuits made up of ideal devices: switches, each with a finite on-state resistance and ideal capacitors. For the basic analysis, the switches have no parasitic capacitances and can be turned on and off arbitrarily with no electrical effort. Also, the capacitors will have no parasitics or series resistance. Parasitics will be considered in section 4 but the fundamental operation of these converters is governed by the output impedance derived in this section.

The output impedance of a switched-capacitor (SC) power converter is dependent on the charge flow

in each capacitor and switch. This important quantity has been calculated using the fundamental cut-set matrix in previous works [4, 10]. If there is only a single input and single output, the charge flow in each capacitor and switch can be expressed as the output charge flow times a constant vector, denoted $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ for capacitors and switches, respectively. These two vectors will be denoted the capacitor charge multiplier vector and the switch charge multiplier vector, respectively, as they multiply the output charge flow to determine the charge flow through each component. The output charge flow is simply the net charge that flows into the output voltage source during a single period in steady-state operation. The charge flows in the capacitors (and similarly, switches) can then be expressed in terms of the output current:

$$\boldsymbol{q_c^j} = \boldsymbol{a_c^j} q_{out} = \boldsymbol{a_c^j} \frac{I_{out}}{f_{sw}} \tag{1}$$

$$\boldsymbol{q_r^j} = \boldsymbol{a_r^j} q_{out} = \boldsymbol{a_r^j} \frac{I_{out}}{f_{sw}} \tag{2}$$

where $\boldsymbol{q_c^j}$ and $\boldsymbol{q_r^j}$ are the capacitor and switch charge flow vectors (respectively) in phase j.

This section has two primary goals. First, a method for determining the $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ vectors without the need for fundamental cut-set matrices will be described. Second, formulas for determining both the slow-switching-limit (SSL) output impedance and the fast-switching-limit (FSL) output impedance directly in terms of the $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ vectors will be derived. These results have not been presented in the past and make the analysis of SC converters significantly easier. In addition, these formulations enable easy component optimization as presented in section 3.

2.1 Determination of the Charge Multiplier Vector by Observation

The charge multiplier vectors $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ can be easily determined by inspection. In this derivation, the $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ vectors for the ladder circuit in figure 2 will be calculated as an example.

The charge multiplier vector for the capacitors will be derived first, assuming all on-state switches are short circuits and all off-state switches are open-circuits. First, the phase 1 and phase 2 networks are drawn, eliminating the switches from the networks. When the switch charge multiplier vector is derived, the switches will be re-incorporated into the networks. These two networks are shown in figure 3.

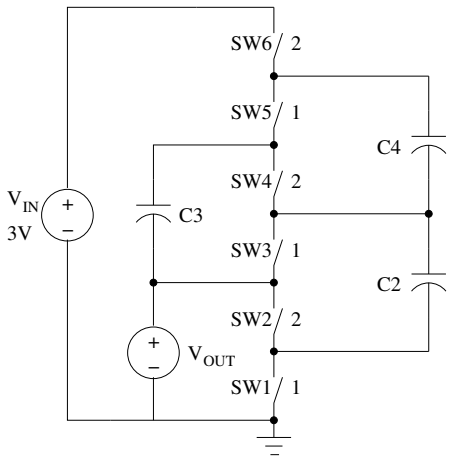
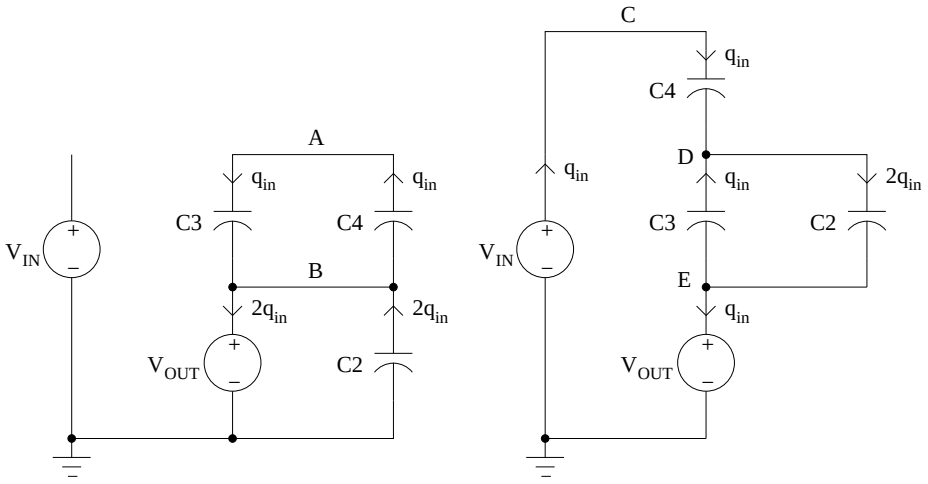


Figure 2: Ladder-type SC converter used in section 2.1



a) phase 1 b) phase 2

Figure 3: Capacitor charge flows

In this circuit, typical of most step-down converters, the input source is connected to the circuit during only one phase (phase 2, in this case). As no charge flows from the input source during phase 1 (in this example), the phase-2 input-source charge flow is defined as q_{in}. Likewise, for most step-up converters, the output source is connected to the converter during only one phase. With such a step-up converter, the output source could serve as a viable starting point for analysis. For the few converters where both sources are connected to the converter during both phases, it may be possible to determine a starting constraint by inspection. If such a constraint does not exist, one can fall back to the matrix-based methods [4] for determining the $\boldsymbol{a_c}$ vector.

From this starting constraint, the capacitor charge flows can be determined using a multi-step approach and Kirchoff's Current Law (KCL). The charge flows in each phase are related since in steady-state operation, the capacitor charge flow in one phase must be equal and opposite to the charge flow in the other phase. In the example circuit, the charge flows are determined iteratively as follows:

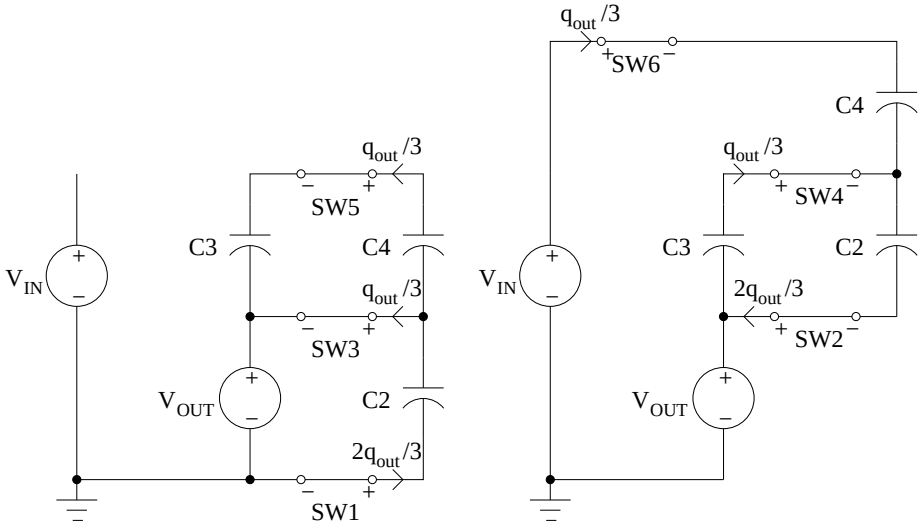
- Phase 2: KCL at node C yields q_{c4}^2: $q_{c4}^2 = +q_{in}$.
- Phase 1: KCL at node A yields q_{c3}^1: $q_{c3}^1 = -q_{c4}^1 = +q_{in}$.
- Phase 2: KCL at node D yields q_{c2}^2: $q_{c2}^2 = -q_{c4}^2 - q_{c3}^2 = +2q_{in}$
- Phase 1: KCL at node B yields q_{out}^1: $q_{out}^1 = +2q_{in}$
- Phase 2: KCL at node E yields q_{out}^2: $q_{out}^2 = +q_{in}$

The sum of the output charge $q_{out} = q_{out}^1 + q_{out}^2$ (over both phases) equals three times the input charge. Thus, the input charge flow equals $q_{out}/3$ and the phase-independent capacitor charge multiplier vector $\boldsymbol{a_c}$ can be obtained:

$$\boldsymbol{a_c} = \begin{bmatrix} a_{c2}^1 \\ a_{c3}^1 \\ a_{c4}^1 \end{bmatrix} = - \begin{bmatrix} a_{c2}^2 \\ a_{c3}^2 \\ a_{c4}^2 \end{bmatrix} = \begin{bmatrix} -2/3 \\ +1/3 \\ -1/3 \end{bmatrix} \tag{3}$$

The input charge flow equals $\boldsymbol{q_{out}/3}$ which indicates that charge is conserved, as the conversion ratio of the converter is 3:1. This check on the input source verifies that the calculation is correct. If one carried out the matrix-based calculations in reference [4], the same result would be obtained.

Next, the switch charge multiplier vector $\boldsymbol{a_r}$ must be computed. In the two networks in figure 3, the closed switches are drawn in and their orientation labeled. This is done for the switches in our example in figure 4.



a) phase 1 b) phase 2

Figure 4: Switch charge flows

Since the charge flows through all the switches are calculated already, the switch charge flows can be represented simply as a linear combination of the capacitor charge flows. By examining the two networks in figure 3 and determining where each closed switch is placed, the networks in figure 4 are found and the charges through the switches calculated using KCL. In the example of the 3-to-1 ladder circuit, the switch charge multiplier vector is given by:

$$\boldsymbol{a_r} = \begin{bmatrix} a_{r1}^1 \\ a_{r2}^2 \\ a_{r3}^1 \\ a_{r4}^2 \\ a_{r5}^1 \\ a_{r6}^2 \end{bmatrix} = \begin{bmatrix} -2/3 \\ -2/3 \\ 1/3 \\ 1/3 \\ 1/3 \\ 1/3 \end{bmatrix} \tag{4}$$

A negative value of $a_{r,i}$ means that if switch i is oriented such that it blocks positive voltage during one

phase, it will conduct negative current during the other phase. Thus, if desired, that switch can be implemented using a passive diode instead of an active switch (if the forward drop is unimportant).

2.2 Slow Switching Limit Output Impedance

A switched-capacitor converter operates in the slow switching limit (SSL) when the switching frequency is sufficiently slow that the charge on each capacitor equilibrates fully during each phase. In the SSL, the currents are modeled as impulsive and the series resistances of the switches, capacitors and interconnects are neglected. In the SSL assumption, these impedances have no effect on the output impedance as they are not large enough to prevent the capacitors from equilibrating fully.

Charge multiplier vectors $\boldsymbol{a^1}$ and $\boldsymbol{a^2}$ will be defined to incorporate the capacitors and voltage sources. In addition to the components in the $\boldsymbol{a_c^1}$ and $\boldsymbol{a_c^2}$ vectors, the multipliers for the input and output charge flows in each phase are included:

$$\boldsymbol{a^1} = \begin{bmatrix} a_{out}^1 \\ \boldsymbol{a_c^1} \\ a_{in}^1 \end{bmatrix} \qquad \boldsymbol{a^2} = \begin{bmatrix} a_{out}^2 \\ \boldsymbol{a_c^2} \\ a_{in}^2 \end{bmatrix} \tag{5}$$

where $q_{in} = a_{in} q_{out} = (a_{in}^1 + a_{in}^2) q_{out}$ and by definition, $a_{out}^1 + a_{out}^2 = 1$.

Given the $\boldsymbol{a^1}$ and $\boldsymbol{a^2}$ vectors, the individual capacitor characteristics and the switching frequency, the SSL output impedance can be calculated. This calculation is based on Tellegen's theorem [11] which states for any network, any vector of branch voltages that satisfies Kirchoff's Voltage Law (KVL) is orthogonal to any vector of branch currents that satisfies Kirchoff's Current Law (KCL). Tellegen's theorem can be applied to both phases of the converter operating in steady state. Both the input and output are modeled as independent voltage sources, but to find the output impedance, the input source voltage is set to zero. The output impedance can then be found by determining the charge flow (or average current) into the non-zero output source.

Since the $\boldsymbol{a^1}$ and $\boldsymbol{a^2}$ vectors each satisfy KCL in their respective phase, Tellegen's theorem yields $\boldsymbol{a^1 \cdot v^1 = 0}$ and $\boldsymbol{a^2 \cdot v^2 = 0}$ for the two respective phases, where $\boldsymbol{v^j}$ represents the asymptotic steady-state

voltage vector during phase j. Adding these two equations, extracting the voltage source components, and noting the input source is shorted yields:

$$v_{out}(a^1_{out} + a^2_{out}) + \sum_{capacitors} (a^1_{c,i} v^1_{c,i} + a^2_{c,i} v^2_{c,i}) = 0 \tag{6}$$

where the first term corresponds to the output voltage source and the terms inside the summation represent each capacitor. By definition, $a^1_{out} + a^2_{out} = 1$ and, by charge conservation in steady-state operation, $a^1_{c,i} = -a^2_{c,i}$. By defining $a_{c,i} = a^1_{c,i} = -a^2_{c,i}$ and $q_i = a_{c,i} q_{out}$ and by multiplying equation (6) by q_{out}, the net charge delivered to the output during a single period, yields:

$$q_{out} v_{out} + \sum_{capacitors} q_i \Delta v_i = 0 \tag{7}$$

where $\Delta v_i = v^1_{c,i} - v^2_{c,i}$. In equation (7), the first term corresponds to the energy supplied by the output source (since the input source is shorted, all dissipated energy must be supplied by the output source) and the terms inside the summation correspond to the per-period energy loss in each capacitor. Unlike the analysis that precedes this work [4], this derivation of the output impedance does not require that capacitor voltages be calculated. The capacitor voltage ripple $\Delta v_{c,i}$ can be computed by:

$$\Delta v_{c,i} = q_i / C_i \tag{8}$$

where C_i is the capacitance of the i^{th} capacitor, assuming linear capacitors. The output impedance calculation also allows the use of nonlinear capacitors, as described at the end of this section.

Substituting equation (8) into equation (7) and dividing by $(q_{out})^2$ yields:

$$\frac{v_{out}}{q_{out}} + \sum_{capacitors} \left(\frac{q_i}{q_{out}} \right)^2 \frac{1}{C_i} = 0 \tag{9}$$

Noting that $\frac{q_i}{q_{out}}$ is the definition of $a_{c,i}$, by dividing (9) by the switching frequency, the average steady-state SSL output impedance is obtained:

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \tag{10}$$

The converter's loss in terms of the series output impedance R_{SSL} can be expressed in terms of capacitor loss. A specific capacitor's loss can be related to its voltage swing during a period. During each period, the

capacitor is charged and discharged between voltages v_1 and v_2, to charge levels q_1 and q_2, respectively, as shown in figure 5. The energy lost during a single period corresponds to:

$$E_{cap} = \Delta v \cdot \Delta q = C\Delta v^2, \tag{11}$$

where the second equality in equation (11) is valid in the case of a standard linear capacitor. The sum of the energy lost through these capacitors is equal to the calculated loss associated with the output impedance for a given load.

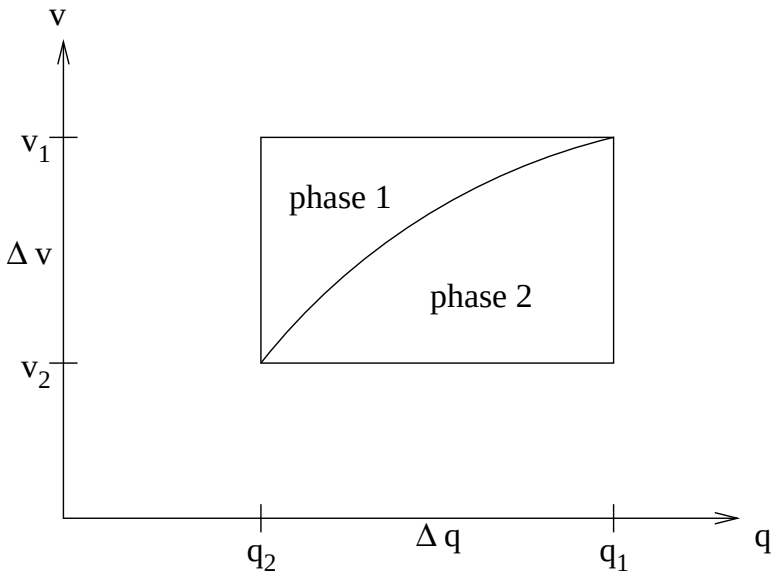


Figure 5: Energy loss due to capacitor charging

This powerful result yields a simple calculation of this asymptotic output impedance and some intuition into the operation of SC converters. The output impedance directly models the losses in the circuit due to capacitor charging and discharging. This impedance can be determined by simply examining the charge flow in the converter without simulation or complicated network analysis.

2.3 Fast Switching Limit Output Impedance

The opposite asymptotic limit, the fast switching limit (FSL), is characterized by nearly-constant current flows between capacitors. The switch on-state impedances and other resistances are sufficiently large such

that during each phase, the capacitors do not approach equilibrium. In the asymptotic limit, the currents between capacitors are constant and capacitor voltages are modeled as constant. The circuit loss is related to conduction loss in resistive elements, independent from the voltage ripple loss of the capacitors. In this section, only the on-state switch resistance will be considered; other parasitic resistance will be considered in section 4.

The duty cycle of the converter is important when considering the FSL impedance since currents flow during the entirety of each phase. The duty cycle of phase 1 will be represented as $D_1 = D$. Likewise, duty cycle of phase 2 will be represented as $D_2 = 1 - D$. Physical implementations will incorporate a non-overlapping clock, but the delay time will be neglected for now. For each switch i, the duty cycle of that switch will be written as D_i where $D_i = D_1$ if switch i is on during phase 1 and $D_i = D_2$ if the switch is on during phase 2. The optimal duty cycle of such a converter is close to 0.5, but due to inherent asymmetries in many topologies, often differs from 0.5 by a slight margin.

The $a_{r,i}$ values derived in section 2.1 represent the charge flow through the switch during the single phase when the switch is on. The values of $a_{r,i}$ are independent of D as they simply represent the charge flow through the switches that ensure charge conservation on the circuit's capacitors. Since the determination of $a_{r,i}$ is single-valued, it cannot change with respect to D while maintaining charge conservation.

In the FSL, the current through the switches (while in the on-state) is assumed to be constant. Given the charge flow vector, the current in each switch is easily determined:

$$i_{r,i} = \frac{q_{r,i} f_{sw}}{D_i} \tag{12}$$

where $q_{r,i}$ is the charge flow through switch i during a single period and D_i is the duty cycle of that switch. Substituting $q_{r,i} = a_{r,i} q_{out}$ and $q_{out} = i_{out}/f_{sw}$ into equation (12) yields:

$$i_{r,i} = \frac{a_{r,i}}{D_i} i_{out} \tag{13}$$

The current through the switches is only dependent on the switch charge multiplier vector, which is obtainable by inspection. The network voltages never need to be found in this analysis, simplifying computation significantly.

The average power loss due to each individual switch is equal to the instantaneous on-state power loss

times its duty cycle. Since the total loss of the SC converter in the FSL is just the sum of the switch losses, the total circuit loss is given by:

$$P_{FSL} = \sum_{switches} D_i R_i \left(\frac{a_{r,i}}{D_i} i_{out} \right)^2 \tag{14}$$

where R_i is the on-state resistance of switch i.

Since the input and output charge in the SC converter is conserved by the conversion ratio n, all the power loss in an ideal SC converter (as analyzed here) is modeled by the output voltage drop. Thus the output impedance can be determined by equating the actual power loss of the circuit with the apparent power loss due to the output impedance. Since this power loss is proportional to the square of the output current, the FSL output impedance can be obtained by inspection:

$$R_{FSL} = \sum_i \frac{R_i (a_{r,i})^2}{D_i} \tag{15}$$

Similar to the SSL output impedance in equation (10), the FSL output impedance is given simply in terms of simple circuit parameters (R_i and D_i) and the switch charge multiplier coefficients of each switch. In the simplified case when the duty cycle for each switch is 50%, the output impedance would be:

$$R_{FSL} = 2 \sum_i R_i (a_{r,i})^2 \tag{16}$$

These two simple forms of the output impedance (given in equations (10) and (15)) can be used to provide strong guidance for the design of switched-capacitor power converters.

3 Optimization of Switched-Capacitor Converters

The performance metrics developed in sections 2.2 and 2.3 enable the development of design guidelines for switched-capacitor (SC) converters. In particular, the output impedance formulas given in equations (10) and (15) enable the optimization of the size of each individual capacitor and switch. These optimizations allow for the better utilization of capacitor energy storage and switch silicon area for a given output impedance.

A typical design process would involve first calculating the $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ vectors for the chosen SC topology. The capacitors would then be chosen optimally according to the procedure in section 3.1. The capacitors are optimized according to the output impedance which depends on the capacitor values, namely the SSL impedance.

Independently from the capacitor optimization, the switches can be optimally sized with respect to each other (section 3.2). This optimization is carried out using the FSL impedance formula, as the FSL impedance depends on switch conductances. Finally, the entire system is considered with respect to the system specifications to choose the minimum total capacitor and switch size. This final step is detailed in section 3.3.

In both the capacitor and switch optimizations, a cost-based constraint is used to ensure the optimal utilization of devices. For the capacitor optimization, the total energy storage capability is held constant, as capacitor energy storage is directly related to physical size and device cost. For the switch optimization, a constraint on the sum of the V-A products over all switches is used, as that metric also represents device cost.

The optimization procedure requires knowledge about the component working voltages, unlike the output impedance analysis. The working voltage for a capacitor is the maximum voltage on the capacitor during steady-state converter operation. For a transistor (switch), the working voltage is the voltage it blocks during steady-state converter operation. These working voltages can be found by inspection. Similar to the method to find the $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ vectors in section 2.1, a multi-step approach is used. Based on the known input source, KVL constraints can be formed to determine the steady-state component voltages. These vectors will be denoted $\boldsymbol{v_c}$ and $\boldsymbol{v_r}$ for the working voltages of the switches and capacitors, respectively.

3.1 Capacitor Optimization

The capacitor optimization uses a constraint that holds the total energy storage capability, summed over all capacitors, fixed to a constant E_{tot}. This constraint can be mathematically expressed as:

$$\sum_i \frac{1}{2}(v_{c,i(rated)})^2 C_i = E_{tot} \tag{17}$$

where C_i represents the value of capacitor i and $v_{c,i(rated)}$ represents the rated voltage of capacitor i. The energy storage capability of a capacitor is related to its rated voltage, as that dictates its size and cost, not the maximum voltage it sees during operation. However, the capacitor's working voltage must be less than the rated voltage to avoid damaging the component, and should be close to the rated voltage to achieve good utilization of the device.

A function $\mathcal{L}$ will be defined to perform the constrained optimization:

$$\mathcal{L} = \sum_i \frac{(a_{c,i})^2}{C_i} + \lambda \left(\sum_i \frac{1}{2}(v_{c,i(rated)})^2 C_i - E_{tot} \right) \tag{18}$$

where the first term represents the SSL output impedance (scaled by switching frequency as it does not effect the minimization) and the second term is proportional to the constraint in equation (17). The impedance will be minimized by equating the partial derivatives of $\mathcal{L}$ with respect to C_i and λ with zero:

$$\frac{\partial \mathcal{L}}{\partial C_i} = -\frac{(a_{c,i})^2}{C_i^2} + \lambda \frac{1}{2}(v_{c,i(rated)})^2 = 0 \tag{19}$$

$$\frac{\partial \mathcal{L}}{\partial \lambda} = \sum_i \frac{1}{2}(v_{c,i(rated)})^2 C_i - E_{tot} = 0 \tag{20}$$

Equation (20) simply repeats the constraint in equation (17).

The relationship in equation (19) sets up a proportionality between C_i and $a_{c,i}$ and $v_{c,i(rated)}$:

$$C_i \propto \left| \frac{a_{c,i}}{v_{c,i(rated)}} \right| \tag{21}$$

This proportionality leads to an expression for the value of each capacitor using the constraint on energy storage:

$$C_i = \left| \frac{a_{c,i}}{v_{c,i(rated)}} \right| \frac{2E_{tot}}{\sum_k |a_{c,k} v_{c,k(rated)}|} \tag{22}$$

The optimal energy storage of each capacitor is proportional to the V-Q product of each capacitor:

$$E_i = \frac{|a_{c,i} v_{c,i(rated)}|}{\sum_k |a_{c,k} v_{c,k(rated)}|} E_{tot} \tag{23}$$

When the total energy is constrained, the optimal capacitor energies are proportional to the product of their rated voltage and their charge multiplier coefficients. In addition, the ripple voltage on each capacitor is directly proportional to that capacitor's rated voltage.

The optimized output impedance can be calculated by combining equations (10) and (22):

$$R_{SSL}^{*} = \frac{1}{2E_{tot}f_{sw}} \left(\sum_{i} |a_{c,i} v_{c,i(rated)}| \right)^{2} \tag{24}$$

By optimizing the capacitors, the output impedance becomes proportional to the square of the sum of the products of voltages and charge flows (V-A product) of each capacitor. The optimization can improve the performance of an SC converter designed in an ad-hoc manner significantly, especially one with a large conversion ratio.

3.1.1 Capacitor Optimization with a single-voltage technology

If all capacitors in a SC converter are rated for the same voltage, the optimization results can be simplified. SC converters built with integrated capacitors often use identically-rated capacitors. In addition, the ladder topology (for example, the converter in figure 2) contains identically-rated capacitors. In this case, we will constrain total capacitance to a value of C_{tot}.

The optimized capacitance (from equation (22)) simplifies to:

$$C_i = \frac{|a_{c,i}|}{\sum_k |a_{c,k}|} C_{tot} \tag{25}$$

Each capacitor is sized proportionally to its charge multiplier coefficient. With optimized capacitors, the voltage ripple on each capacitor is set equal in magnitude.

The optimized SSL output impedance (from equation (24)) thus simplifies to:

$$R_{SSL}^{*} = \frac{1}{C_{tot}f_{sw}} \left(\sum_{i} |a_{c,i}| \right)^{2} \tag{26}$$

These optimization results for the single-voltage technology are very simple to utilize in switched-capacitor converter design.

3.2 Switch Optimization

Like capacitors, the switches in a SC converter can be optimized, yielding dramatic performance increases. This optimization is carried out in the asymptotic fast switching limit where output impedance is directly related to switch conductance. While it is possible to include duty cycle optimization in this calculation, it does not affect the optimal values noticeably and significantly complicates the analysis. Thus, this optimization will use a duty cycle of 50% and the FSL output impedance given by equation (16).

A cost-based constraint will be used to obtain the lowest output impedance for a given cost. Most discrete MOS-type transistors are characterized (and their cost established) according to their V-A product. The optimization should hold cost, represented by the sum of the V-A product for all switches, constant. This V-A metric corresponds to a constraint on the G-V^2 product summed over the switches.

In an integrated application, the same total G-V^2 constraint applies. The transistor length and nominal voltage scale linearly with process generations. In addition, switch conductance scales inversely to transistor length. This constraint can be visualized by considering unit switch blocks, each supporting one volt and having a conductance of one unit (ie. siemens). To increase the conductance of a switch, multiple blocks must added in parallel. To increase the rated voltage, blocks must be added in series (to increase the blocking voltage) and in parallel (to keep the conductance the same). Thus, the area required to create a transistor with conductance G that blocks voltage V would be $A_{sw} = GV^2$ (in units of GV^2, ie. S-V^2).

This constraint, applicable to both discrete and integrated transistors, can be expressed as:

$$A_{tot} = \sum_{switches} G_i (v_{r,i(rated)})^2 \tag{27}$$

where G_i is the conductance of switch i and $v_{r,i(rated)}$ is the rated voltage of switch i. Similar to the capacitor optimization, $v_{r,i(rated)}$ is the voltage the device can support, not necessarily the voltage it blocks in normal operation. Naturally, the rated voltage must be larger than the nominal blocking voltage.

A Lagrange optimization function $\mathcal{L}$ will be formed to minimize the FSL output impedance while satisfying the constraint:

$$\mathcal{L} = \sum_i \frac{(a_{r,i})^2}{G_i} + \lambda \left(\sum_{switches} G_i (v_{r,i(rated)})^2 - A_{tot} \right) \tag{28}$$

The first term corresponds to the FSL output impedance (the constant in equation (16) does not affect the optimization) and the second term corresponds to the constraint in equation (27). The minimization is performed by taking the partial derivative of equation 28 with respect to G_i and setting it to zero:

$$\frac{\partial \mathcal{L}}{\partial G_i} = -\frac{(a_{r,i})^2}{G_i^2} + \lambda (v_{r,i(rated)})^2 = 0 \tag{29}$$

Again, differentiating with respect to λ yields the constraint in equation (27).

Equation (29) directly yields a relation between G_i and the switches' charge multiplier coefficient and their voltage rating:

$$G_i \propto \frac{|a_{r,i}|}{v_{r,i(rated)}} \tag{30}$$

This proportionality, in addition to the $G - V^2$ constraint in equation (27), yields an expression for the conductance of each switch:

$$G_i = \frac{1}{R_i} = \left| \frac{a_{r,i}}{v_{r,i(rated)}} \right| \frac{A_{tot}}{\sum_k |a_{r,k} v_{r,k(rated)}|} \tag{31}$$

Comparing the optimal conductance G_i to the optimal capacitance in equation (22) makes it evident that the two optimizations are closely related.

The optimal FSL output impedance is obtained by substituting equation (31) into the FSL output impedance equation (equation (16)):

$$R_{FSL}^* = \frac{2}{A_{tot}} \left(\sum_i |a_{r,i} v_{r,i(rated)}| \right)^2 \tag{32}$$

Similar to the optimal SSL impedance, the optimal FSL output impedance is related to the square of the sum of the V-A products. This simple form of the optimal output impedance allows us to consider and compare various SC converter topologies. Several SC converter topologies will be compared in section 3.4. This switch optimization can improve the performance of switched-capacitor converters, especially ones with large conversion ratios if designed in a ad-hoc method.

3.2.1 Switch Optimization for Single-Voltage Switches

Many SC converters use switches with a single voltage rating. For instance, most IC-based converters will only use the native NMOS transistors of the process since they are the best-performing transistors.

In addition, topologies such as the ladder converter utilize switches that must all block the same voltage. The switch-cost constraint discussed in the previous section simplifies into a constraint on total switch conductance G_{tot}.

The optimal switch conductance G_i in equation (31) simplifies to:

$$G_i = \frac{|a_{r,i}|}{\sum_k |a_{r,k}|} G_{tot} \tag{33}$$

likewise, when all switches are rated for an identical voltage, the optimal FSL output impedance simplifies to:

$$R^*_{FSL} = \frac{2}{G_{tot}} \left(\sum_i |a_{r,i}| \right)^2 \tag{34}$$

The performance of a converter is related to the square of the sum of the charge multiplier coefficients. Topologies with a small sum of these coefficients will perform better for a given switch conductance than a topology with a large sum of coefficients. In integrated applications or other applications where a single-voltage switches must be used, this optimization can be used. A comparison of SC converters based on single-voltage devices is performed in section 3.4.

3.3 System Optimization

The optimal SSL and FSL output impedance asymptotes derived in sections 3.1 and 3.2 define the performance of a SC DC-DC converter over the spectrum of switching frequencies. The output impedance bode plot can be modeled as a pole-zero system as shown in figure 6, but is not precisely accurate. The actual frequency characteristics must be calculated using matrix-based state-space models. However, the simple asymptotic model is sufficiently accurate for converter design, optimization and control.

Most design specifications include an output voltage drop at maximum load (which translates to maximum-load efficiency). This drop defines a nominal output impedance R_{NOM} at a maximum load current I_{LOAD}. Based on the technology used to implement the converter, the device parasitics govern the maximum practical switching frequency (these parasitics are described in section 4). At the maximum load, the converter should be designed to operate at this frequency (denoted f_{max}). The optimal design involves placing the crossover frequency f_z (the switching frequency where the SSL and FSL output impedances are equal) at

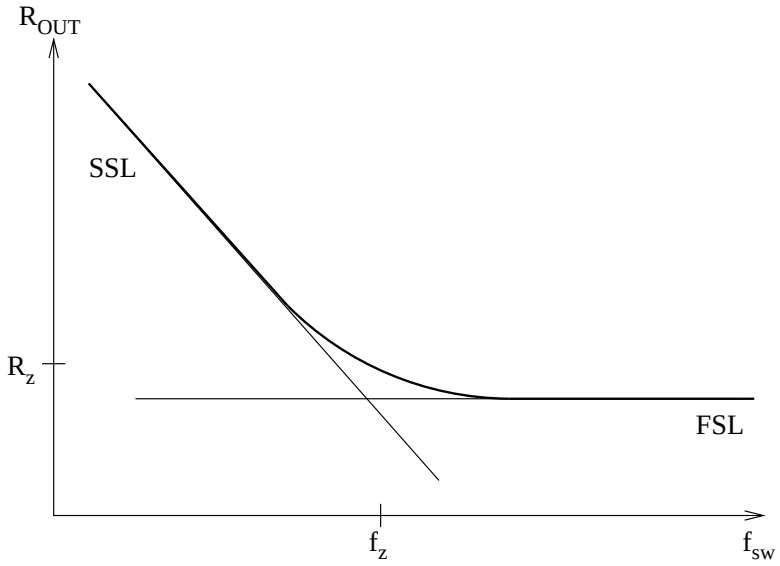


Figure 6: Output impedance vs. switching frequency

the maximum switching frequency f_{max}.

This design method involves sizing the capacitors and switches such that the SSL and FSL output impedances both equal $R_{NOM}/\sqrt{2}$ at switching frequency f_{max}. When the impedances are set to these values, the total output impedance at that frequency would approximately equal the nominal impedance R_{NOM}. For lighter loads, the switching frequency can be backed off to obtain a higher output impedance but lower parasitic loss.

This design method is shown to be optimal by examining changes in the component values. If either the switches or capacitors are made significantly smaller, the desired output impedance could not be obtained for any switching frequency less than f_{max}. If the switches are made larger than necessary, parasitic loss would increase as the switching frequency would remain constant (as it is capacitor-dependent at that point). On the other hand, if the capacitors are made larger, the switching frequency could be decreased to achieve the same output impedance, but the cost associated with the capacitors would increase as well. This design procedure results in the converter with the smallest-size (and thus, lowest cost) devices that meets the design specifications.

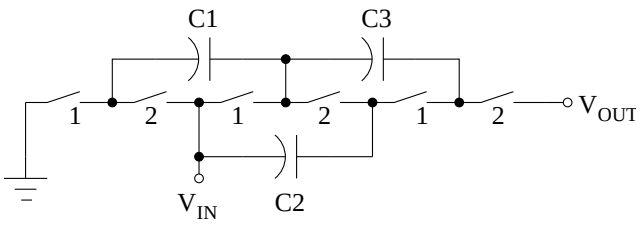
3.4 Comparison of Topologies

A number of SC converter topologies exist in literature, but the merits of each have never been compared in a methodical way. The optimizations in sections 3.1 and 3.2 can be used to provide a performance comparison between different common SC converter topologies. Figure 7 shows five converter topologies discussed in the literature.

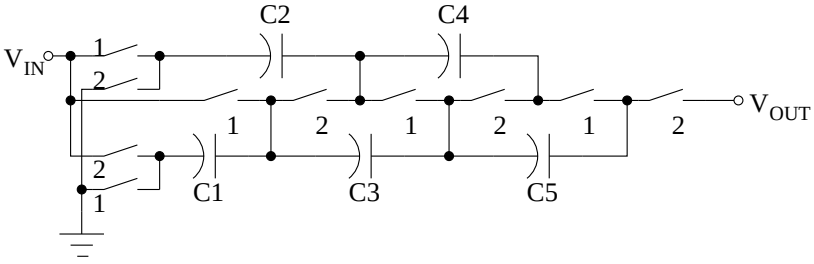
The first comparison will assume device cost scales as described in sections 3.1 and 3.2. Thus, devices of every voltage rating are available and can there are no disadvantages for using any voltage device. Step-up versions of the topologies will be considered (as shown in figure 7, although step-down versions would yield identical results. The optimal output impedance for all topologies in both asymptotic limits will be evaluated. An input voltage of 1 volt will be assumed, and a range of conversion ratios (represented by n) will be considered. The calculations for each individual topology are summarized following the comparison.

When evaluating the FSL output impedance, the converters will be evaluated on the ratio $\frac{V_{OUT}^2/R_{FSL}}{A_{tot}}$ (the ratio between the G-V^2 product of the converter and the G-V^2 product summed over all switches). For a given cost constraint and conversion ratio, the converter with the highest metric will be the one with the lowest output impedance. Likewise, when the SSL output impedance is considered, the converters will be evaluated on the ratio $\frac{V_{OUT}^2/R_{SSL}}{E_{tot}f_{sw}}$. For a given total capacitor energy storage, the topology with the highest metric will have the lowest SSL output impedance.

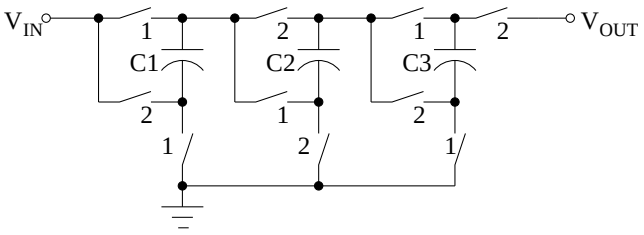
After performing the optimization and comparison, the five topologies are compared in figure 8. At a conversion ratio of two, all topologies perform identically. Upon further inspection, for $n = 2$, these five topologies are topologically identical. Converters that do well in the SSL comparison, such as the series-parallel topology, do poorly in the FSL comparison. Conversely, topologies such as the Dickson Charge Pump and the Ladder topology that perform well in the FSL comparison typically perform poorly in the SSL comparison. Exponential converters, such as the Fibonacci and Doubler topology do reasonably well in both cases. Some converters use capacitors efficiently and others use switches efficiently, but no converters use both optimally. For converters designed using a capacitor-limited process, a series-parallel topology would work best, while switch-limited designs should use a topology such as the Dickson charge pump or ladder topology.



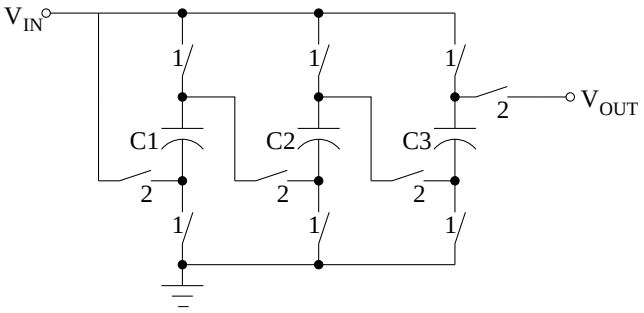
a) Ladder



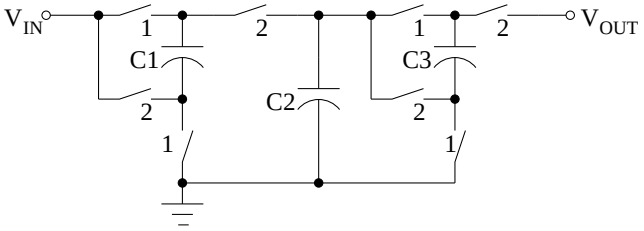
b) Dickson Charge Pump



c) Fibonacci

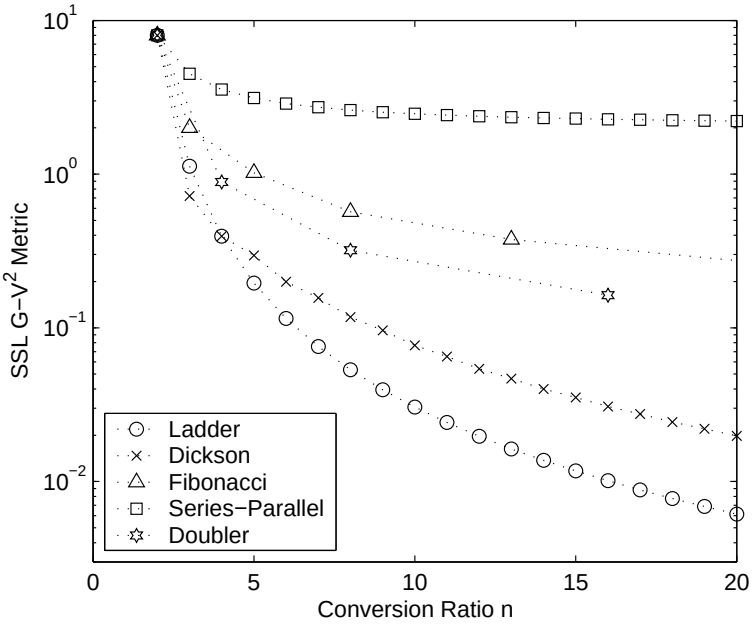


d) Series-Parallel

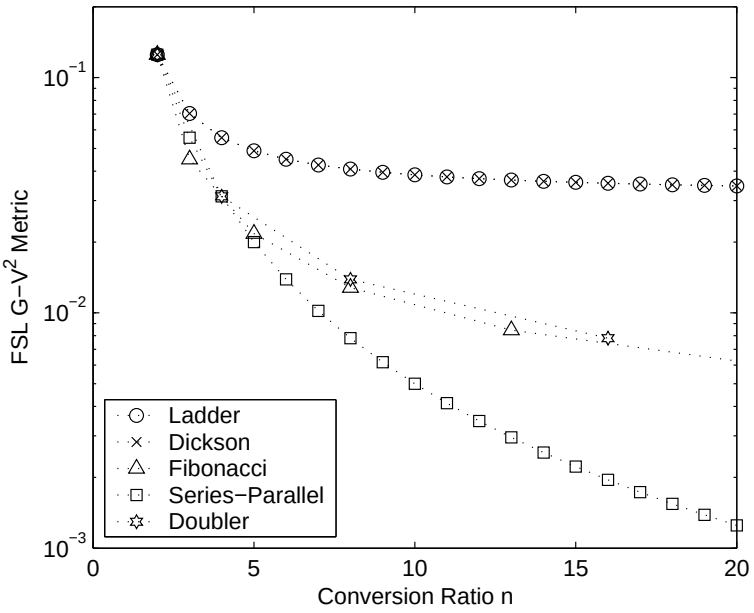


e) Doubler

Figure 7: Five common switched-capacitor converter topologies (step-up form)



(a)



(b)

Figure 8: (a) SSL and (b) FSL performance metrics with optimal-voltage devices

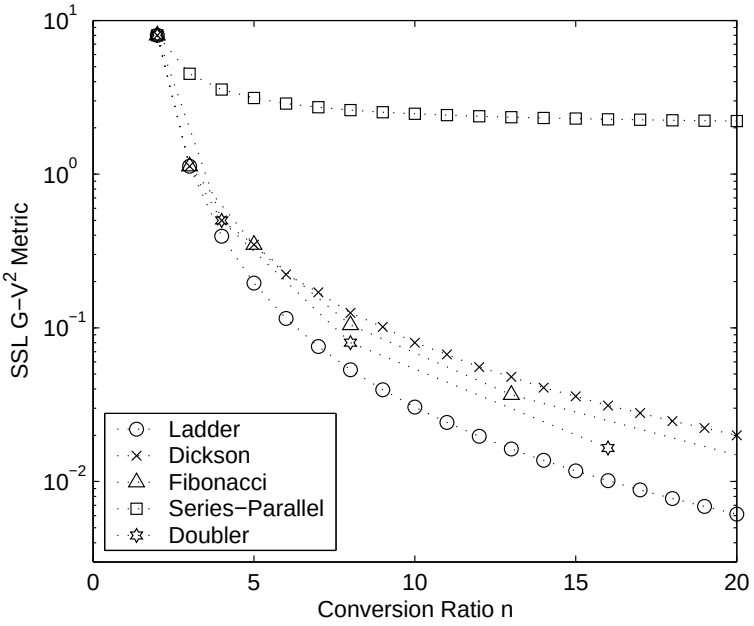
The exponential converters, such as the Fibonacci and Doubler topologies, seem to perform reasonably well in both the SSL and FSL comparisons. However, since the switches and capacitors used in their implementations are of all different voltage levels and most of the switches are not ground-referenced, practical implementation would be difficult if not impractical. The second comparison performed assumes that all devices must be of the same voltage rating. In integrated applications using standard CMOS processes, the switches and capacitors are usually all rated for the same voltage. The process is chosen such that this voltage rating corresponds to the maximum voltage seen on any device. However, the switches and capacitors can be rated differently from each other, ie. if the highest-voltage switch is rated for 1 volt, a 1 volt process would be used, even if some capacitors support a higher voltage. The same comparison metrics will be used as were used in the previous comparison.

The comparison results using identically-rated switches and transistors are shown in figure 9. The series-parallel topology is still optimal in the SSL comparison, as all capacitors in that topology also support the same voltage. Likewise, the ladder topology is optimal in the FSL comparison, as all switches in that topology support the same voltage. However, the exponential converters are poor in both comparisons because they use a wide range of devices, which is impractical in implementation. These comparisons can be used to select the best topology for any given application.

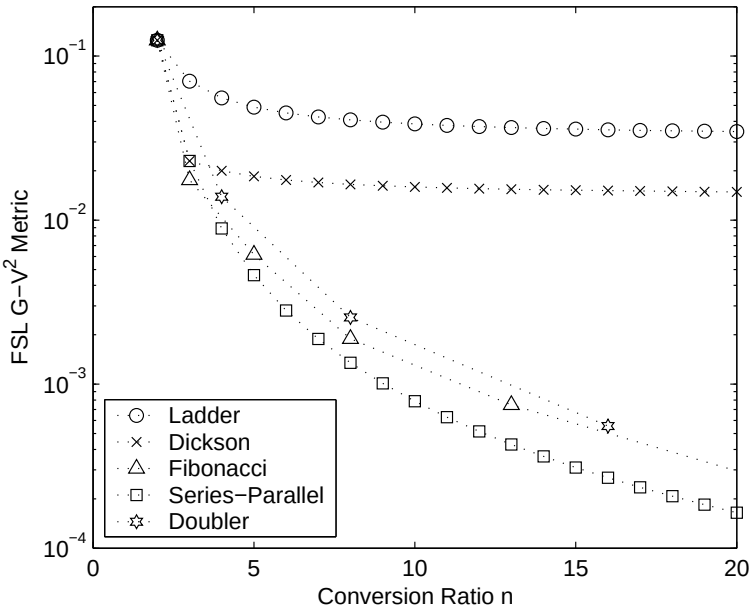
Algebraic formulations and asymptotic limits of the output impedance for the topologies are useful in comparison. The four relevant sums (shown in equations (24), (26), (32) and (34)) are calculated for a general conversion ratio n. In addition, four output impedances are calculated. R_{SSL1} and R_{FSL1} are the SSL and FSL output impedances for the first assumption that devices of all voltage ratings are available. Second, R_{SSL2} and R_{FSL2} will be calculated assuming that only one voltage device exists (the second assumption).

3.4.1 Ladder Topology

The ladder topology [10] is based on two sets (or ladders) of capacitors. For these calculations, the step-up converter will be considered, but the step-down version yields identical results. One set forms a chain from ground (including the input and output voltage sources). These capacitors hold a set of DC potentials at



(a)



(b)

Figure 9: (a) SSL and (b) FSL performance metrics with single-voltage devices

integer multiples of the input or output voltage (for step-up or step-down converters, respectively). The other set of capacitors (referred to as the flying capacitors) shuttle charge between the DC-referenced capacitors to equalize them. Each capacitor (by inspection) supports the input voltage (set to equal 1 volt, without loss of generality). The charge multiplier vector $\boldsymbol{a_c}$ is given by:

$$\boldsymbol{a_c} = \begin{bmatrix} 1 & 1 & 2 & 2 & 3 & 3 & \cdots & (n-2) & (n-1) \end{bmatrix}^\top \in \mathcal{R}^{2n-3} \tag{35}$$

The sums of the components of the relevant vectors for optimization can be expressed as a function of the conversion ratio n:

$$\sum_i a_{c,i} v_{c,i} = \sum_i a_{c,i} = (n-1)^2 \tag{36}$$

Thus, the optimized SSL output impedance is given by:

$$R_{SSL1} = \frac{(n-1)^4}{2 f_{sw} E_{tot}} \tag{37}$$

where the total energy storage quantity E_{tot} is normalized to one. Since the maximum voltage on any switch is 1 volt, the optimized output impedance when the total capacitance is normalized to one is:

$$R_{SSL2} = \frac{(n-1)^4}{f_{sw} C_{tot}} \tag{38}$$

Similarly, the switches each support a volt and most of the switches have a charge multiplier coefficient of 1, although the bottom two switches have a multiplier coefficient of $(n-1)$:

$$\boldsymbol{a_r} = \begin{bmatrix} (n-1) & (n-1) & 1 & 1 & 1 & 1 & \cdots \end{bmatrix}^\top \in \mathcal{R}^{2n} \tag{39}$$

In terms of n, the sum of the products between switch charge multiplier coefficients and voltages yields:

$$\sum_i a_{r,i} v_{r,i} = \sum_i a_{r,i} = 4(n-1) \tag{40}$$

Thus, when the total V-A product constraint and the total switch conductance constraint are set to one, the FSL output impedance of the ladder topology is given by:

$$R_{FSL1} = \frac{32}{A_{tot}} (n-1)^2 \tag{41}$$

$$R_{FSL2} = \frac{32}{G_{tot}} (n-1)^2 \tag{42}$$

3.4.2 Dickson Charge Pump

The Dickson charge pump [5, 8, 9] has a similar structure to the ladder topology in that it has two ladders of capacitors. However, in this topology, both ladders move with respect to ground. The pair of base inverters (see figure 7b) cause each ladder to move up and down an amount equal to the input voltage. Since they move in opposing directions, the ladder steps are in multiples of twice the input voltage, not just one like the ladder topology. Thus, all the capacitors and switches, except for one lowest capacitor (C1 in figure 7b) and the inverter switches must be rated for twice the input voltage. The lowest capacitor and the inverter switches must be rated for only the input voltage. For a conversion ratio of 2, unneeded switches can be removed to create a converter topologically equivalent to the ladder.

The capacitor voltage and charge multiplier vectors, based on the above explanation, are given by:

$$\boldsymbol{v_c} = \begin{bmatrix} 1 & 2 & 2 & 2 & 2 & \cdots & 2 \end{bmatrix}^\top \in \mathcal{R}^{n-1} \tag{43}$$

$$\boldsymbol{a_c} = \begin{bmatrix} floor\left(\frac{n}{2}\right) & \cdots & 3 & 3 & 2 & 2 & 1 & 1 \end{bmatrix}^\top \in \mathcal{R}^{n-1} \tag{44}$$

For a given conversion ratio n, the sum of the capacitor charge multiplier coefficients and the sum of the product of the capacitor charge multiplier coefficients and their voltage components can be found:

$$\sum_i a_{c,i} = floor\left(\frac{n^2}{4}\right) \tag{45}$$

$$\sum_i a_{c,i} v_{c,i} = floor\left(\frac{n^2}{2} - 1\right) \tag{46}$$

These sums yield the optimized output impedance under both comparisons. Note that the maximum voltage on any capacitor is two volts in this topology (except when $n = 2$, which is not included in the following expressions).

$$R_{SSL1} = \frac{\left(floor\left(\frac{n^2-2}{2}\right)\right)^2}{2E_{tot}f_{sw}} \approx \frac{(n^2-2)^2}{8E_{tot}f_{sw}} \tag{47}$$

$$R_{SSL2} = \frac{(floor(n^2/2))^2}{C_{tot}f_{sw}} \approx \frac{n^4}{4C_{tot}f_{sw}} \tag{48}$$

Similarly, the appropriate sums for the switches can be obtained using similar methods. The inverter switches must carry approximately half the input charge flow, but support only one volt, while the other

switches carry much less current, but support two volts. These sums can be found exactly in terms of n:

$$\sum_i a_{r,i} = 3n - 2 \tag{49}$$

$$\sum_i a_{r,i} v_{r,i} = 4n - 4 \tag{50}$$

The output impedance using both constraints can easily be computed in terms of the previously-computed sums:

$$R_{FSL1} = \frac{32}{A_{tot}}(n-1)^2 \tag{51}$$

$$R_{FSL2} = \frac{8}{G_{tot}}(3n-2)^2 \tag{52}$$

Again, since the $n = 2$ converter reduces to the ladder form, it will not satisfy equation (52). The impedance in equation (52) is worse than that in equation (42) since the inverter switches are not being used to their full potential when all switches must be made in the same voltage technology.

3.4.3 Fibonacci Topology

The Fibonacci topology, discussed in depth in reference [4], provides the largest conversion ratio for a given number of capacitors. Using k capacitors (not including the input and output capacitor), a conversion ratio of $n = F_{k+2}$ can be obtained, where k is a positive integer. For instance, with 3 capacitors, a conversion ratio of 5 can be obtained. The j-th Fibonacci number, for $j \geq 1$ can be expressed as:

$$F_j = \frac{\phi^j - (1-\phi)^j}{\sqrt{5}} = \{1, 1, 2, 3, 5, 8, 13, \cdots\} \tag{53}$$

where ϕ is the golden ratio ($\phi = (1+\sqrt{5})/2 = 1.618...$).

The charge multiplier vector and supporting voltage vector of the capacitors is given by:

$$\boldsymbol{a_c} = \begin{bmatrix} F_k & \cdots & 8 & 5 & 3 & 2 & 1 & 1 \end{bmatrix}^\top \in \mathcal{R}^k \tag{54}$$

$$\boldsymbol{v_c} = \begin{bmatrix} 1 & 2 & 3 & 5 & 8 & 13 & \cdots & F_{k+1} \end{bmatrix}^\top \in \mathcal{R}^k \tag{55}$$

For a given conversion ratio n, the sum of the capacitor charge multiplier coefficients and the sum of the product of the capacitor charge multiplier coefficients and their voltage components can be found:

$$\sum_i a_{c,i} = F_{k+2} - 1 \tag{56}$$

$$\sum_i a_{c,i} v_{c,i} = \sum_{i=1}^{k} F_i F_{k+2-i} \tag{57}$$

where k and n are related by $F_{k+2} = n$. The convolution in equation (57) is difficult to express in a closed form, but this sum grows exponentially with respect to k. The output impedance under both assumptions can be found:

$$R_{SSL1} = \frac{\left(\sum_{i=1}^{k} F_i F_{k+2-i}\right)^2}{2E_{tot} f_{sw}} \tag{58}$$

$$R_{SSL2} = \frac{F_{k+1}^2 (F_{k+2} - 1)^2}{C_{tot} f_{sw}} \tag{59}$$

The second output impedance (R_{SSL2}) is increased by a factor of F_{n+1}^2, where F_{k+1} is the maximum voltage on a capacitor in that topology.

Similarly, the appropriate sums for the switches can be obtained using similar methods. Similar to the capacitors, the switches also support some voltage which is included in the Fibonacci sequence:

$$\boldsymbol{a_r} = \begin{bmatrix} F_{k+1} & F_k & \cdots & 2 & 2 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}^\top \in \mathcal{R}^{3k+1} \tag{60}$$

$$\boldsymbol{v_r} = \begin{bmatrix} 1 & 1 & 1 & 2 & 2 & 1 & \cdots & F_{k+1} & F_{k+1} & F_k & F_k \end{bmatrix}^\top \in \mathcal{R}^{3k+1} \tag{61}$$

The relevant sums are difficult or impossible to compute in a closed-form expression. For the latter sum, the sequence of results for $n = \{2, 3, 4...\}$ is provided instead. It can be found by taking the inner product of the $\boldsymbol{a_r}$ and $\boldsymbol{v_r}$ vectors.

$$\sum_i a_{r,i} = 3(F_{k+2} - 1) + F_{k+1} \tag{62}$$

$$\sum_{\boldsymbol{i}} \boldsymbol{a_{r,i} v_{r,i}} = \begin{Bmatrix} 4 & 10 & 24 & 50 & 100 & \cdots \end{Bmatrix} \tag{63}$$

The output impedance using both constraints can be computed in terms of the previously-computed sums:

$$R_{FSL1} = \frac{1}{A_{tot}} \begin{Bmatrix} 32 & 200 & 1152 & \cdots \end{Bmatrix} \tag{64}$$

$$R_{FSL2} = \frac{2}{G_{tot}} F_{k+1}^2 \left(3(F_{k+2} - 1) + F_{k+1}\right)^2 \tag{65}$$

Since the maximum voltage on any switch is given by F_{k+1}, the output impedance R_{FSL2} is scaled by F_{k+1}^2 to account for technology scaling. Note that while these impedances increase exponentially, the conversion ratio n also increases exponentially.

3.4.4 Series-Parallel Topology

The series-parallel topology [3, 2, 7] implements a step-up converter by, in phase one, connecting all $n-1$ capacitors in parallel to the input source. In phase two, the capacitors are connected in series with each other and the input source to deliver charge to the output. Its simple operation and efficient utilization of capacitors makes it favorable for low-voltage designs, but with high-voltage designs, the switches are difficult to drive and each must support a different voltage.

The series-parallel topology's good use of capacitors result in each capacitor having an $a_{c,i}$ of one and a $v_{c,i}$ component of one. For a given conversion ratio n, the sum of the capacitor charge multiplier coefficients and the sum of the product of the capacitor charge multiplier coefficients and their voltage components can be found exactly:

$$\sum_i a_{c,i} = \sum_i a_{c,i} v_{c,i} = n - 1 \tag{66}$$

With these simple expressions for the relevant sums, the two appropriate output impedances can be found:

$$R_{SSL1} = \frac{(n-1)^2}{2E_{tot} f_{sw}} \tag{67}$$

$$R_{SSL2} = \frac{(n-1)^2}{C_{tot} f_{sw}} \tag{68}$$

The switches on the other hand, while they still have a charge multiplier coefficient of $a_{r,i} = 1$, must support higher voltages. The appropriate sums to find output impedance can be found exactly in terms of n:

$$\sum_i a_{r,i} = 3n - 2 \tag{69}$$

$$\sum_i a_{r,i} v_{r,i} = n^2 + n - 2 \tag{70}$$

The output impedance using both constraints can easily be computed in terms of the previously-computed sums:

$$R_{FSL1} = \frac{2}{A_{tot}} (n^2 + n - 2)^2 \tag{71}$$

$$R_{FSL2} = \frac{2}{G_{tot}} (n-1)^2 (3n-2)^2 = 2(3n^2 - 5n + 2)^2 \tag{72}$$

Since the maximum voltage supported by any switch in the circuit is $n-1$ volts, the R_{FSL2} impedance is penalized appropriately. When compared to the ladder or Dickson charge pump topologies, the series-parallel excels in capacitor usage but suffers when switch usage is considered.

3.4.5 Doubler Topology

The doubler topology is made up of an integer number of doubling stages. For example, the converter in figure 7e consists of two doubling stages. Each stage doubles the voltage and uses two capacitors and four switches. The last doubling stage only uses one capacitor, as the output capacitor is that stage's second capacitor and is ignored in this computation. For a given integer k, the conversion ratio of the circuit is given by $n = 2^k$.

The doubler structure yields a regular pattern for the $a_{c,i}$ and $v_{c,i}$ quantities:

$$\boldsymbol{a_c} = \begin{bmatrix} 2^{k-1} & \cdots & 4 & 2 & 2 & 1 & 1 \end{bmatrix}^\top \in \mathcal{R}^{2k-1} \tag{73}$$

$$\boldsymbol{v_c} = \begin{bmatrix} 1 & 2 & 2 & 4 & 4 & \cdots & 2^{k-1} \end{bmatrix}^\top \in \mathcal{R}^{2k-1} \tag{74}$$

For a given k and conversion ratio $n = 2^k$, the sum of the capacitor charge multiplier coefficients and the sum of the product of the capacitor charge multiplier coefficients and their voltage components can be found:

$$\sum_i a_{c,i} = \frac{3n}{2} - 2 \tag{75}$$

$$\sum_i a_{c,i} v_{c,i} = (2k-1)\frac{n}{2} \tag{76}$$

With these simple expressions for the relevant sums, the two SSL output impedances can be derived:

$$R_{SSL1} = \frac{n^2(2k-1)^2}{8E_{tot}f_{sw}} \tag{77}$$

$$R_{SSL2} = \frac{(3n^2-4n)^2}{4C_{tot}f_{sw}} \tag{78}$$

Each switch in a single stage supports that stage's input current and its output charge flow. The appropriate sums to find output impedance can be found exactly in terms of n:

$$\sum_i a_{r,i} = 4(n-1) \tag{79}$$

$$\sum_i a_{r,i} v_{r,i} = 2nk \tag{80}$$

The output impedance using both constraints can easily be computed in terms of the previously-computed sums:

$$R_{FSL1} = \frac{8}{A_{tot}} n^2 k^2 \tag{81}$$

$$R_{FSL2} = \frac{8}{G_{tot}}(n^2 - n)^2 \tag{82}$$

Since the maximum voltage on any switch is half the output voltage, the output impedance is penalized accordingly. Thus, the doubler topology only provides benefits when the technology can support multiple voltage ratings.

3.5 Comparison with Conventional DC-DC Converters

Switched-capacitor converters have several advantages over conventional inductor-based DC-DC converters. With a switched-capacitor converter, conduction and switching losses are not additional losses, but are already incorporated in the output impedance based losses calculated in sections 2.2 and 2.3. The only losses that are not included in the output impedance are the gate drive (and other parasitic) losses and control power. Short-circuit (shoot-through) power can be eliminated by the use of sufficiently non-overlapping clocks. Stray capacitances from dynamic nodes must be minimized and their losses incorporated into the efficiency of the converter if the strays are not eliminated. These losses and implementation details will be further considered in section 4.

A SC converter and a conventional DC-DC converter can be compared directly when the conduction loss is considered. The silicon area (for the switches and control functions) is the dominant cost in many DC-DC converters. A converter with a significantly-lower switch loss may have a cost advantage over a converter with a higher switch loss. For the SC converter, the conduction loss is equal to the loss corresponding to the FSL output impedance. The conduction loss of an inductor-based converter is equal to or greater than the resistive losses occuring in the on-state resistances of the switches. Because the FSL is considered, a ladder-type step-up converter (such as the one in figure 7a) will be used, as it (along with the Dickson charge pump) uses switches most efficiently. Two magnetic-based converters will be considered, the boost converter and transformer-bridge converter, both shown in figure 10. Total switch G-V^2 product will be held constant for all converters, and the SC converter will be assumed to operate in the FSL. Finally, all switches will be sized optimally based on the optimization methods presented in this paper. All converters have a step-up ratio of n and an input voltage of 1 volt.

The step-up ladder-type SC converter will be considered first. All switches in the ladder topology must

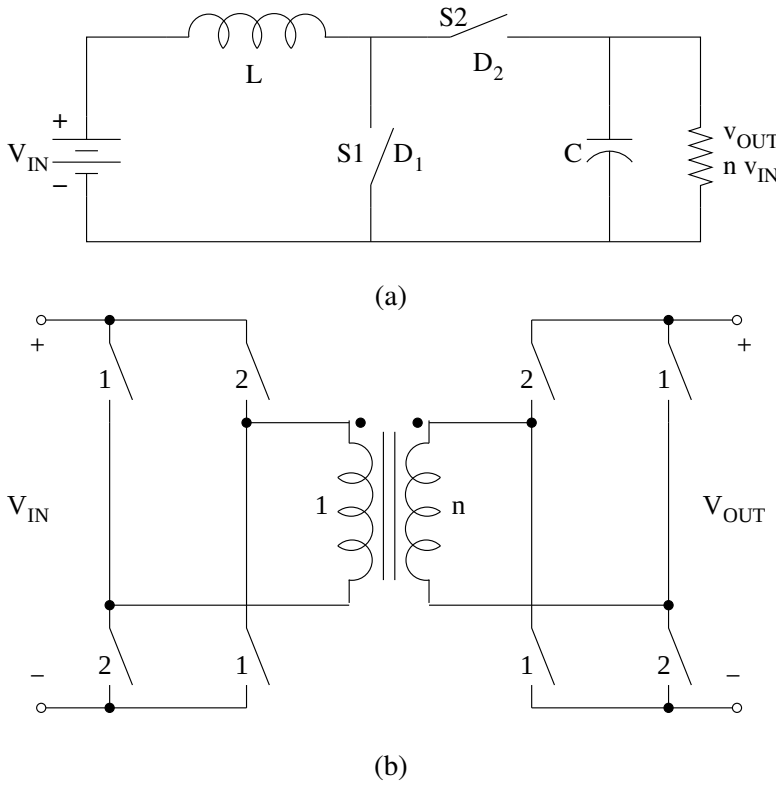


Figure 10: (a) Standard Boost Converter (b) Transformer-Bridge Converter

be rated for 1 volt. The lowest two switches in the ladder structure have an a_r component of $(n-1)$ while the other $2(n-1)$ switches simply have an a_r component of 1. Thus, the sum of the a_r components is:

$$\sum_i |a_{r,i}| = 2(n-1) + 2(n-1) = 4(n-1) \tag{83}$$

The optimal FSL output impedance of this converter (normalized such that $A_{tot} = 1$) is thus:

$$R_{out} = 2\left(\sum_i |a_{r,i} v_{r,i(rated)}|\right)^2 = 32(n-1)^2 \tag{84}$$

This result was previously computed in section 3.4.1

The boost converter in figure 10a is operated at duty cycle $D = 1/n$ to achieve a step-up ratio of n. The duty cycle of switch S1 is $D_1 = D = 1/n$ and the duty cycle of switch S2 is $D_2 = 1 - D = (n-1)/n$. The conduction loss in this circuit is directly obtainable as:

$$P_{cond} = \left(\frac{D}{G_1} + \frac{1-D}{G_2}\right) I_{in}^2 = R_{out} I_{out}^2 \tag{85}$$

The equivalent loss impedance R_{out} can be directly compared to the output impedance of the SC converter. Optimizing the ratio of the two switch conductances for a given duty cycle, the following constraint can be derived:

$$\left(\frac{G_1}{G_2}\right)^2 = \frac{D}{1-D} \tag{86}$$

Since the total G-V^2 product of the switch is constrained at one and each switch in the boost converter must be rated for the output voltage of n, the total conductance is restricted to $G_{tot} = 1/n^2$. From this constraint, the equivalent loss impedance can be determined (note that $D = 1/n$ to achieve the correct conversion ratio):

$$R_{out} = n^2\left(\frac{D}{G_1} + \frac{1-D}{G_2}\right) = n^2\left(1 + 2\sqrt{\frac{n-1}{n^2}}\right) \tag{87}$$

Finally, the transformer-based direct converter in figure 10b will be considered. The transformer is assumed to be ideal and to have an up-conversion ratio of n. The output switches are all identical and must be rated for the output voltage of n. The on-current of these switches is equal to the output current I_{out}. Likewise, the input switches must be rated for 1 volt and conduct a current of nI_{out}. All of these 8 switches thus have a V-A product of 1. To keep the total G-V^2 product equal to one, the output switches must have conductances of $1/8n^2$ and the input switches must have conductances of $1/8$. The conduction loss can be

calculated as:

$$P_{cond} = 2(8n^2)\left(\frac{I_{out}}{n^2}\right)^2 + 2(8)I_{out}^2 = 32I_{out}^2 \tag{88}$$

The equivalent loss impedance is a constant 32 ohms in this case, which makes intuitive sense as only the ideal transformer is changed to achieve different conversion ratios.

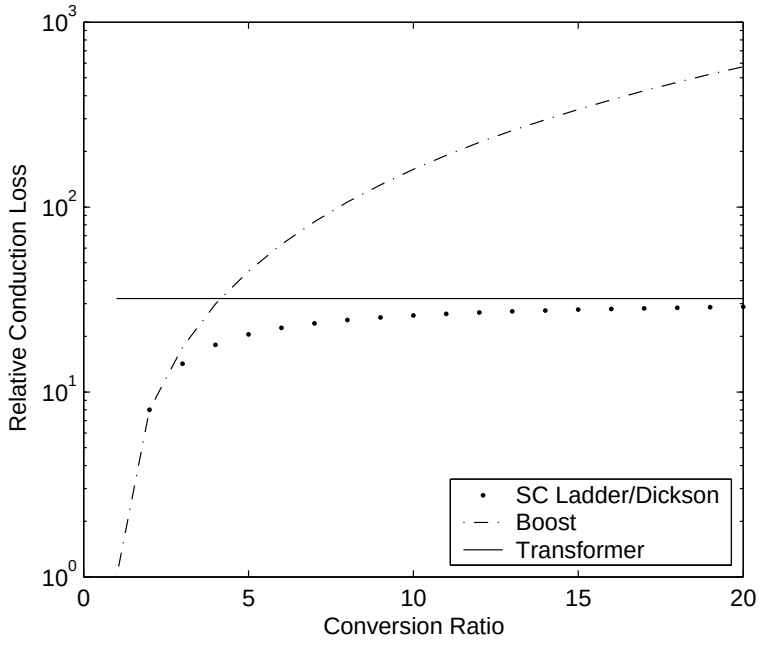


Figure 11: Conduction Loss Comparison

The three conduction losses (represented by equivalent power-loss output impedance) are compared and the results are plotted in figure 11. The SC and boost converters' output impedance increases as the conversion ratio increases, but the SC converter approaches an asymptotic limit at $R_{out} = 32$ (the same as the transformer-based converter).

At large conversion ratios, the ladder-type SC converter is significantly superior to the boost converter as the switches in the ladder topology block only the input voltage and most switches carry less than the input current. However, the boost converter's switches carry the full input current and block the full output voltage. Even though the SC converter has many more switches, the low V-A product of these switches yields a lower conduction loss than the boost converter, with its much higher V-A product switches.

At a conversion ratio of 2, the performance of the SC converter equals that of the boost converter. At

lower conversion ratios, the boost converter is superior as it is operating near its optimal point (a duty-cycle of one). The SC converter reaches its simplest form at a conversion ratio of 2. For conversion ratios between 1 and 2, more switches and capacitors are necessary, compared to the $n = 2$ case. The analysis for such converters is not performed here, but can be performed easily through the methods developed here.

In an application where switches are the limiting factor in performance or cost, switched-capacitor converters are evidently advantageous over conventional magnetics-based DC-DC converters at high or moderate conversion ratios.

4 Implementation Considerations

Implementing a switched-capacitor (SC) DC-DC converter using either discrete or integrated components takes some consideration. SC converters require more care than a standard buck or boost converter due to the number of components (especially switches) involved in the design. First, implementation of a high-voltage converter in a modern CMOS process will be discussed. The losses due to parasitic capacitance will be calculated and used to put an effective limit on switching frequency. Next, capacitor implementations will be considered including integrated and external ceramic capacitors. Capacitor losses due to coupling and ESR will be calculated.

4.1 Implementation in CMOS

Integration is advantageous for switched-capacitor converters as they are often used for low-power applications. The control, gate drive and power switches can all be included on the same die, simplifying manufacturing and assembly compared to inductor-based converters. However, ICs typically only have one or two optimal transistor voltages, making it difficult to implement topologies with a wide range of switch voltages. There are two general implementation strategies for an IC-based SC converter.

High-voltage converters are implemented using a ladder or Dickson charge pump topology where the process transistors support the lower of the input or output voltage. Other topologies cannot be used, as the transistors would not be able to support some of the switch voltages occurring in those topologies. An example of such a converter is a 12 volt to 1 volt converter using a modern 0.13 μm or 0.25 μm CMOS process. Each transistor must support 1 volt (or 2 volts for the Dickson charge pump), but no individual device needs to support the 12 volt input. A triple-well or silicon-on-insulator (SOI) process must be used such that NMOS transistors can be built with a bulk terminal at any arbitrary potential. PMOS power transistors are avoided as they have inferior mobility and would require significantly more chip area compared to a NMOS-based design. In addition, floating NMOS transistors are required for most gate drive methods, as presented in section 4.2.

Low-voltage converters can be implemented with any topology. In this case, all voltages seen in the

circuit are less than the process voltage. Although the switches cannot be fully optimized in this case (since their voltage rating is excessive), the series-parallel topology or an exponential-type topology may be used to minimize device sizes. An example of such a converter would be a 500mV to 100mV converter using a 90 nm process. Any topology can be used as no switches would support more than the rated voltage of the process. It is still important to drive the transistors with the highest drive level possible to improve conduction. These converters do not need a triple-well or SOI process, as all NMOS power transistors can be made with the same bulk with only a moderate penalty.

4.2 Gate Drive Techniques

When implementing a high-voltage converter, controlling the gates of the transistors is an important consideration. In the ladder and Dickson charge pump topologies, transistors are stacked to form a ladder where each *rung* supports the rated voltage of the process. For some step-up converters, these switches can be implemented as diodes, but the diode drops will severely limit the performance of the converter. Thus, these transistors must be actively driven from circuits running at the MOSFET transistors'source potential.

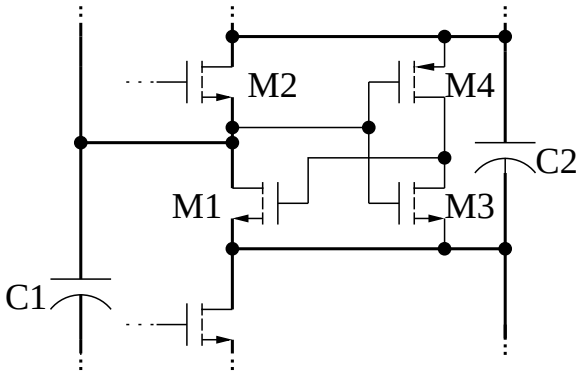


Figure 12: Latch-based gate drive

Several gate drive schemes have been developed for FLASH memory supplies [5, 8, 9]. Such a drive circuit is shown in figure 12. These circuits utilize a latch-type structure to create a bistable drive. The drive for transistor M1 is powered from the voltage on capacitor C2, which will provide the ideal supply for driving the gate of M1. Likewise, the drive for the power transistor below M1 will be supplied by C1. Assuming M1 and M2 are driven with a complementary signal – M1 is off when M2 is on and vise-versa –

M1 and M2 will form an inverter. M3 and M4 form an inverter as well, and these two inverters are partially cross-coupled, forming a latch. The bottom transistor in the chain is ground referenced, and the next-lowest transistor has a source at nearly ground potential. These two devices are driven directly from the system clock. These transitions carry up the ladder, causing all transistors to switch into the desired phase after some transient period.

Although this structure has been used in many applications [5, 8], it is not ideal for medium- to high-power converters. Cross-coupled inverters, during a state transition, incur a large short-circuit current. Since one of these inverters is made with the main power transistors, the short-circuit current is likely to be huge and intolerable. In addition, since the latches will only change states at the rising edge of each phase, the deadtime between phases will essentially be eliminated. Thus, additional current will flow between switches of opposite phase. This current will connect capacitor networks of different voltages, which will partially discharge the storage capacitors. For converters handling any sort of power, these currents will seriously reduce the efficiency of the converter, and should be avoided.

The use of switched-capacitor converters for medium to high power, high-voltage applications requires the use of an efficient gate-drive method. Since each rung of the ladder structure blocks the rated voltage of the process, a level-shifter is needed to drive each gate. In addition, each phase of the converter must be driven independently to ensure a deadtime to eliminate short-circuit current. Finally, any latching functions must be built with small devices such that the short-circuit current associated with the control is minimal. After some research, a cascode-based level-shift gate drive was developed, similar to the digital level-shifter in [6]. This gate drive method is shown in figure 13.

Similar to the latch-based gate drive, the gate drive for each transistor is supplied from the capacitor connected to the transistor's source. The core of the cascode level-shift gate drive is the cross-coupled inverter pair. It is minimum-sized and is supplied locally (for instance, by capacitor C2 for the gate drive of M2). It is pulled to ground on either side by transistors M6 and M9 and the connections to the lower gate drive circuit. It is only controlled from the lower gate drive cell, not the upper one, and can be turned on and off independently. Cascode PMOS transistors M6 and M9 protect the inputs of the inverters from being pulled too low (and breaking down the inverters' PMOS transistors). Likewise, cascode NMOS transistors M11 and M12 (similarly, M5 and M8) protect transistors M7 and M10 from a high drain voltage. M7 and

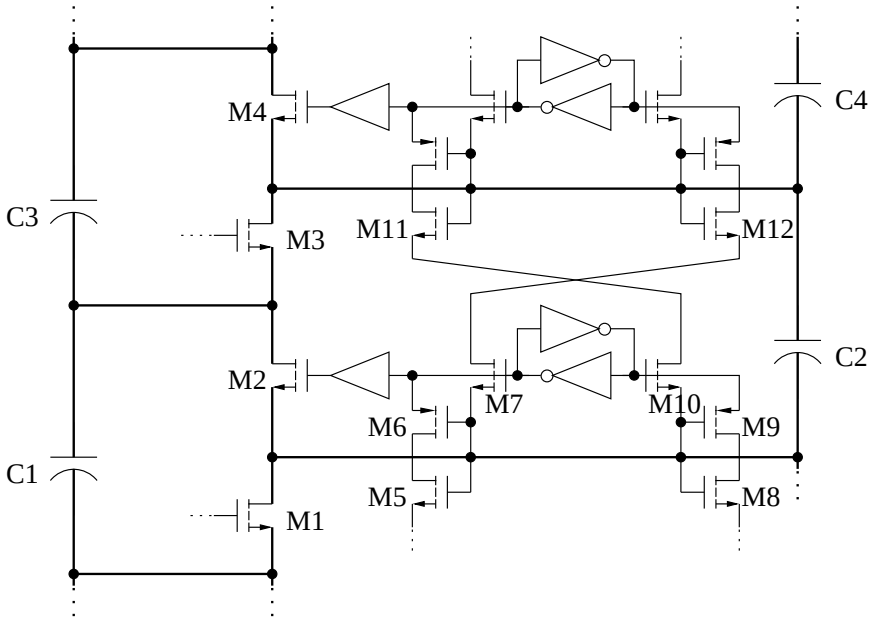


Figure 13: Cascode level-shift gate drive

M10 amplify the control signals and send them to the next gate drive cell. A buffer finally drives the large power transistor M2. This gate drive scheme solves many of the problems of the latch-based gate drive while only moderately increasing the complexity of the drive. Verification of this design through simulation is discussed in section 6.2.

4.3 MOSFET Parasitic Capacitance Loss

MOSFET transistors have a number of associated parasitics which negatively affect performance of switched-capacitor (SC) converters. There are three primary losses associated with the transistors in the circuit, all related to charging and discharging parasitic capacitors. These losses are all proportional to switching frequency and are also proportional to the conductance (or area) of the switches. These relationships will be considered in section 4.6.

The primary parasitic loss is due to the gate capacitance. This capacitance must be fully charged and discharged every period. The voltage it is charged to is not inherent to the converter topology, but is a func-

tion of the gate drive and the technology used to implement the transistors. To improve switch conductance, the gate drive voltage should be as large as possible given the technology limits. The gate capacitance is nonlinear, but since it is charged between two fixed limits (zero and V_{GS} volts, where V_{GS} volts is the drive voltage for that specific implementation), the capacitance can be linearized to C_{GS}. The capacitor is linearized by finding the slope of the chord connecting the points on the Q-V characteristics defined by the two gate voltage levels. In other words, since the gate is charged between 0 volts and V_{GS} volts, the linearized capacitance is given by $C_{GS} = Q_G(V_{GS})/V_{GS}$. The power loss due to this capacitance is given by:

$$P_{Cgs} = f_{sw} \sum_i C_{GS,i} V_{GS,i}^2 \tag{89}$$

where $C_{GS,i}$ is the gate-source capacitance of switch i and $V_{GS,i}$ is the drive voltage of that switch.

The next substantial parasitic capacitance loss is the drain-bulk capacitance of each transistor (where the bulk (or well) potential is typically the same as the source potential). This capacitance must also be charged and discharged every period, but its voltage is determined from the network. The off-state drain-bulk voltage on each transistor is given by $v_{r,i}$, which is determined by inspecting the converter topology. The drain-bulk capacitance is also nonlinear, but since it is charged between two voltage levels (0 and $v_{r,i}$), it can also be linearized to C_{DB}, similar to the gate-source capacitance. The power loss due to this capacitance is given by:

$$P_{Cdb} = f_{sw} \sum_i C_{DB,i} (v_{r,i})^2 \tag{90}$$

where $C_{DB,i}$ is the linearized drain-bulk capacitance of transistor i.

Finally, there is a power loss due to the source-substrate or bulk-substrate capacitance. This loss is only applicable to the transistors where the source is not at a DC potential with respect to ground. In a standard CMOS process, this capacitance is between a transistor's source and substrate and can be expressed as $C_{BS,i}$ (which would equal zero for transistors with DC-biased sources). If implemented using a triple-well process, this capacitance would be the linearized capacitance of the well junction (between the bulk and substrate). If an SOI process was used, this capacitance is negligible. In some topologies, such as the ladder converter, the voltage these flying transistors swing over is equal to their drain-source voltage $v_{r,i}$, since half the transistors have a DC-referenced source. In general, this voltage can be represented as $v_{bs,i}$. The power loss due to this

source-bulk capacitance is given by:

$$P_{Cbs} = f_{sw} \sum_i C_{BS,i} (v_{bs,i})^2 \tag{91}$$

The three losses discussed in this section penalize large switches and high switching frequencies, as these losses are proportional to switching frequency and switch area. Thus, the optimal total switch size (when concerned with power loss) is the smallest that satisfies the constraints in section 3.3.

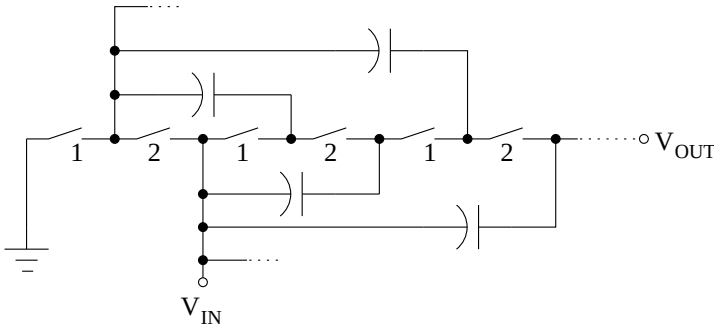
4.4 Capacitor Implementation

Two types of capacitors are popular in switched-capacitor (SC) DC-DC converter applications. For low-power applications, integrated capacitors are convenient and help create an ultra-compact final product. If a higher power level is needed, external ceramic capacitors can be used for their relatively-low ESR and far-superior capacitance compared to integrated capacitors. With either capacitor technology, several design considerations exist.

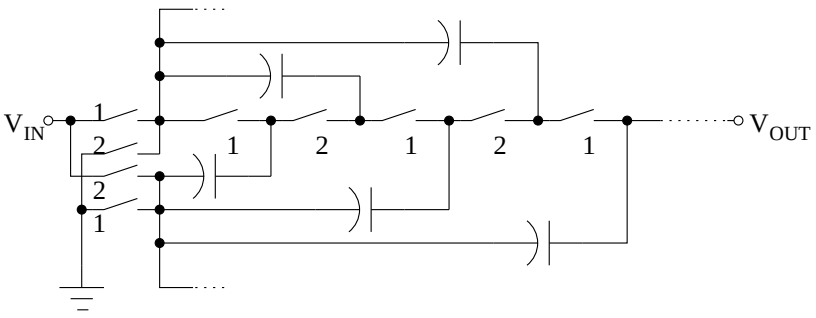
Large integrated capacitors are notoriously difficult to implement. The oxide capacitance yields the largest capacitance per area, but it is highly nonlinear and, additionally, oxide capacitors have a high coupling capacitance to the substrate. These losses will be discussed in sections 4.5.2 and 4.5.3. Other integrated capacitors are often more ideal, but have a very poor energy density, so their utility is limited to ultra-low-power applications. Some specialized processes offer a high-metal layer high-density capacitor with a reasonable energy density and low parasitics. These capacitors should be used if they exist, as they provide superior performance. Since integrated capacitors usually support a low voltage, a SC converter topology that features low per-capacitor voltages should be used.

If discrete ceramic capacitors are used, considerable power levels can be achieved efficiently. Small surface-mount packages can be used that feature high energy densities and low equivalent series resistances (ESRs). Other technologies, such as tantalum or electrolytic capacitors, offer better energy densities, but their ESR-per-volume ratios are poor compared to ceramic capacitors, so they offer no significant advantages. High-value ceramic capacitors often have large voltage coefficients. The effects corresponding to this voltage coefficient are discussed in section 4.5.3. Ceramic capacitors have a much higher energy den-

sity at higher voltage ratings, so topologies that utilize capacitors that block a high voltage should be used. The ladder and Dickson charge pump topologies in figure 7 usually utilize low-voltage capacitors, but the capacitors can be re-arranged to support higher voltages. The corresponding $a_{c,i}$ values decrease, leading to an advantage in implementation. The switch configuration and ratings remain the same. These modified topologies are shown in figure 14.



a) Ladder



b) Dickson Charge Pump

Figure 14: Discrete-capacitor versions of SC converters

4.5 Capacitor Losses

Several capacitor-induced power losses exist in switched-capacitor power converters. These losses were discussed briefly in section 4.4. The ESR loss applies to both types of capacitors (integrated and discrete) but is more important in high-power converters with external capacitors. The ground-coupling loss is significant only when using integrated capacitors. However, the pad-to-ground capacitance when using discrete capacitors is also considered a ground-coupling capacitance. Finally, the voltage coefficient loss is important when

considering gate oxide integrated capacitors and high-k discrete capacitors.

4.5.1 Capacitor ESR Loss

The capacitor ESR loss is equal to the conduction loss through each capacitor's equivalent series resistance. This loss can be modeled using the FSL output impedance tools developed in section 2.3. The charge multiplier coefficient for each capacitor's ESR is equal to the capacitor's $a_{c,i}$, since they both support the same charge flow. However, the capacitor supports (equal) charge flow during each phase, so the contribution to the FSL occurs during both phases. The FSL output impedance, including ESR contribution, is given by:

$$R_{FSL} = R_{FSLo} + \sum_i R_{ESR,i}(a_{c,i})^2 \left(\frac{1}{D} + \frac{1}{1-D}\right) \tag{92}$$

$$= R_{FSLo} + 4\sum_i R_{ESR,i}(a_{c,i})^2 \tag{93}$$

where R_{FSLo} is the switch-only FSL impedance, given in equation (15) and $R_{ESR,i}$ is the ESR (in ohms at the switching frequency) of capacitor i. Equation (93) holds when the duty cycle is 50%. This ESR contribution to the output impedance is added directly to the FSL output impedance and is not frequency-dependent, unlike the other parasitic loss terms.

4.5.2 Ground Coupling Loss

The ground coupling loss is attributable to integrated capacitors and pad-to-ground capacitance. Integrated capacitors have a parasitic capacitance between the bottom plate of the capacitor and the substrate which ranges between 1% and 30% of the capacitor value, depending on the capacitor technology used. The pad capacitance is mostly attributed to the junction capacitance of the ESD diodes and will vary with pad voltage. Let this coupling capacitance (for capacitor i) equal $C_{gnd,i}$ (linearized if necessary).

This loss only affects flying capacitors – ones that do not have ground-referenced terminals (in steady-state). In the ladder topology (in figure 14), only half the capacitors are flying, as the other half form a string of capacitors from a DC voltage. The Dickson charge pump topology, however, contains all flying capac-

itors. Let $\Delta v_{cdc,i}$ be the voltage potential swing between the terminals of the capacitor and ground. Since the voltage on the capacitor remains roughly constant in steady state under normal operating conditions, the voltage swing of both terminals is approximately equal. The power loss due to this coupling capacitance is given by:

$$P_{cap,gnd} = f_{sw} \sum_i C_{GND,i} \Delta v_{c,gnd,i}^2 \tag{94}$$

where $C_{gnd,i}$ is the total linearized ground coupling capacitance for both terminals of capacitor i.

4.5.3 Capacitor Voltage Coefficient Loss

High-value ceramic capacitors often have high voltage coefficients along with their high dielectric constants. Thus, when they support a higher voltage (as would be optimal for a SC converter), their capacitance would decrease. This effect would only contribute to an increase in the SSL impedance. This revised output impedance can be calculated using equation (10) for the voltage-coefficient adjusted capacitance.

If the voltage-charge characteristics (such as those shown in figure 5) exhibit hysteresis, additional SSL power loss is expected. This power loss would be attributed to the energy represented by the additional area in the curve in figure 15. This power loss can be factored into the SSL impedance as additional $\Delta v \Delta q$ loss.

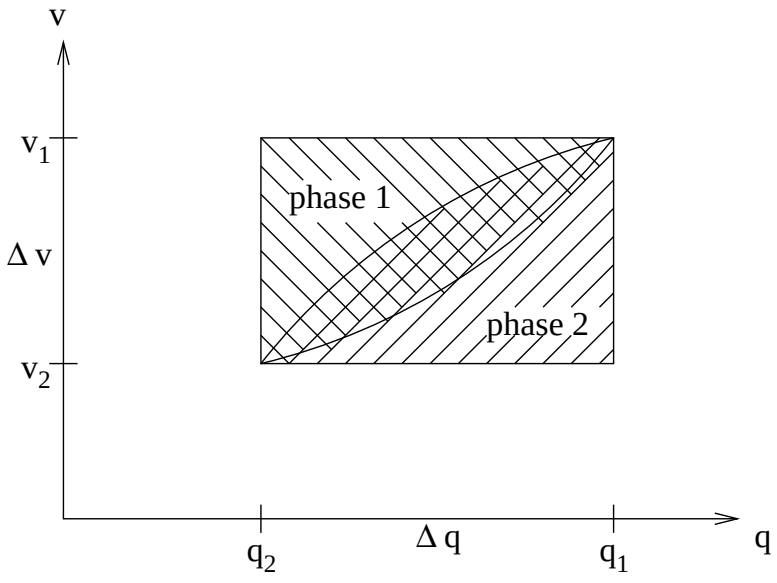


Figure 15: Additional energy loss due to capacitor hysteresis

4.6 Parasitic-Constrained Performance Limits

The majority of the components of parasitic power loss are proportional to switching frequency. However, the ESR loss is constant and can be added to the FSL output impedance. Similarly, the voltage coefficient losses are inversely related to switching frequency, and can be added to the SSL output impedance. These two loss factors will be neglected in the remainder of this section. The remainder of the terms can be grouped into one switching-frequency-dependent power loss term:

$$P_{HF} = f_{sw}\left[\sum_{switches}\left(C_{GS}V_{GS,i}^2 + C_{DS,i}(v_{r,i})^2 + C_{SB,i}(v_{sb,i})^2\right) + \sum_{capacitors} C_{GND,i}(\Delta v_{c,gnd,i})^2\right] \quad (95)$$

Note that this power loss is independent of output load current and is just related to parasitic capacitances, steady-state voltage levels and switching frequency. This power loss can be used to set an upper limit to the practical switching frequency of any SC converter. Once this power equals the output impedance power, given by $P_Z = R_{OUT}i_{out}^2$, there is little reason to increase the switching frequency further. A *power-loss impedance* can be defined to characterize the power loss of a SC converter:

$$R_{PWR} = R_{OUT} + \frac{P_{HF}}{i_{out}^2} \quad (96)$$

where R_{OUT} is the SSL and/or FSL output impedance derived in sections 2.2 and 2.3. P_{HF} is the parasitic power loss discussed above.

To decrease the effects of the parasitic power loss, the switching frequency should be decreased while maintaining the same output impedance. The switch parasitics are proportional to switch area and thus are proportional to switch conductance. To compensate for parasitic loss, the capacitors must be made larger to allow for a lower switching frequency and parasitic loss. If the FSL impedance was made lower instead, the parasitic loss would increase as the switch conductances increase.

5 Control Methods

Regulation in a DC-DC converter is an important part of its functionality. Conventional DC-DC converters are regulated by varying the duty cycle. For switched-capacitor converters, varying the duty cycle has little effect on the output voltage. The output voltage is fundamentally determined by the topology of the converter and little can be done to drastically change the characteristics of the converter. However, there are two major methods of providing regulation in a SC converter. The first method changes the switching frequency based on load to absorb the appropriate voltage drop in the output impedance. The second method involves switching the input or output between different points in a converter to obtain different conversion ratios. The two methods can be combined to form an effective control scheme for a SC power converter.

5.1 Switching-Frequency-Based Control

The output voltage of a SC converter can be regulated over a small range below the nominal output voltage by the use of frequency modulation. Since the output impedance of a converter when operating in the SSL is frequency dependent, the switching frequency can be changed to vary the output impedance. This impedance can be used to drop the necessary voltage between the nominal output voltage (a rational multiple or divisor of the input voltage) and the desired output voltage. The power associated with this voltage drop (and the output current) is dissipated inside the converter. Efficiency-wise, this regulation method is equivalent to using an LDO (low-dropout regulator) in series. At low voltage drops, this is an effective way of providing regulation but becomes inefficient and impractical for a large range of voltage regulation.

One regulation method may use a linear feedback loop to control the switching frequency in terms of the output voltage. Current feedforward (from the output current) can be used to control the switching frequency with feedback to adjust for small errors in the feedforward. The transient response can be improved greatly by using feedforward. However, since the transient response of the system is frequency-dependent, the system is nonlinear. The control system is especially stressed when the load varies by several orders of magnitude. This load variation is common in switched-capacitor designs as SC converters handle large load transients well. A converter can work well over many decades of load power by simply varying the switching

frequency. However, designing a linear controller to handle a wide range of load currents is difficult. Thus, a nonlinear control method may provide superior results.

Hysteretic feedback can be used to control the output voltage with minimal control circuitry. In addition, hysteretic feedback is guaranteed to be stable. However, the method yields a substantially larger (and lower-frequency) output ripple and a poor output spectrum. Two switching frequency levels f_{hi} and f_{lo} are defined. Frequency f_{hi} is sufficiently high to provide a sufficiently high output voltage for any load condition. Likewise, f_{lo} is sufficiently low to supply any expected load at the correct output voltage. Frequency f_{lo} could even equal zero – the converter would be turned off. The hysteretic controller switches between these two frequency levels to keep the voltage on the output capacitor between two hysteresis levels v_{hi} and v_{lo}. These voltages are defined to be slightly higher and slightly lower than the desired output voltage. When the output voltage exceeds v_{hi}, the switching frequency is set to f_{lo}. Likewise, when the output voltage falls below v_{lo}, the switching frequency is increased to f_{hi}. The output voltage then stays within a fixed range of the desired output voltage. A MATLAB^{TM} simulation of this control method was performed and the waveforms are shown in figure 16.

The simulation incorporates a simplified model of the SC converter which neglects switching-frequency-based ripple. The load current is varied over three discrete levels and the converter responds appropriately by varying the switching frequency between two discrete limits (set to 1 and 16 megahertz). The voltage is regulated within a hysteresis band between 2.09 and 2.11 volts.

Hysteretic control can be implemented simply (using two comparators, a RS-latch and a few other circuits) and provides a well-regulated output voltage. There is an upper-limit to the switching frequency (exactly equaling f_{hi}) so the gate drive and delay can be tuned to this maximum switching frequency. Finally, no efficiency losses can be attributed to this control method. The average switching frequency using hysteretic control is equal to the optimal switching frequency for a given output current, assuming the circuit is not operating in the FSL at frequency f_{hi}. Thus, there are no additional gating or parasitic losses associated with hysteretic control, as those losses are proportional to switching frequency. Hysteretic control is a simple and effective method of performing frequency-based output regulation when a low output ripple is not needed.

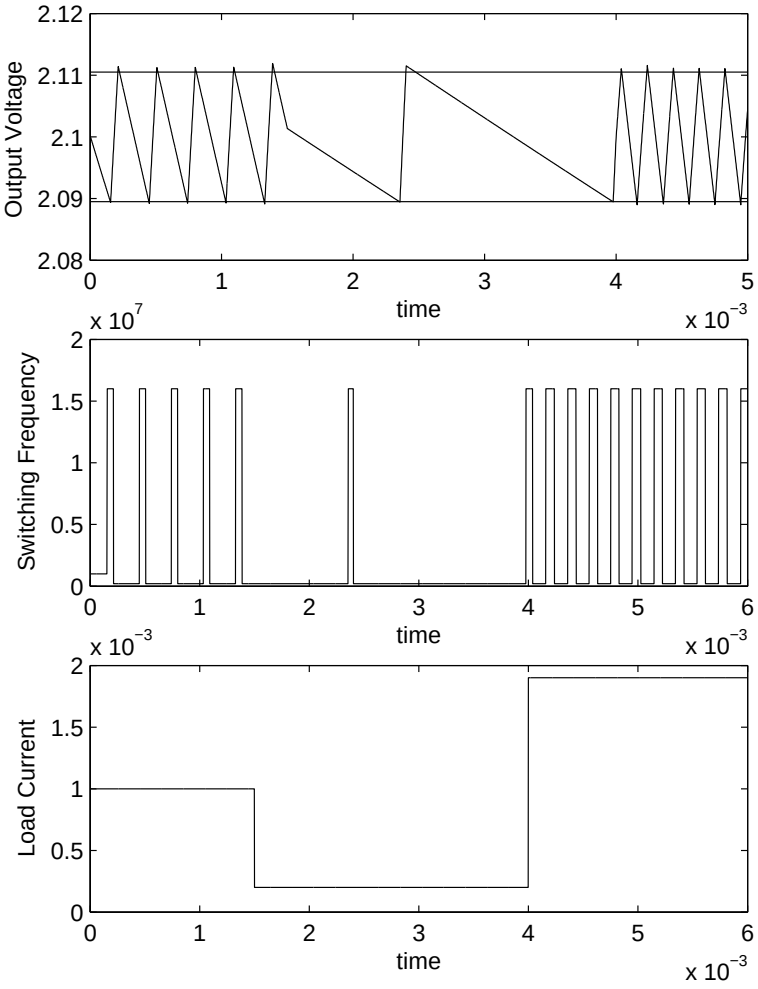


Figure 16: Hysteresis control simulation

5.2 Switched-Input Control

If large variation in the input voltage or desired output voltage are expected, additional control methods must be employed. Switching frequency modulation is useful for regulation over a small range, but if regulation must be performed efficiently over a significant input or output range, the topology must be modified to provide several conversion ratios. In some topologies, the switch phasing can be modified to provide different conversion ratios [4]. In the ladder and Dickson charge pump structures, the input or output tap (for step-down and step-up converters, respectively) can be changed dynamically to provide several discrete step-up or step-down ratios. A step-down version of the ladder topology using this control method is shown in figure 17.

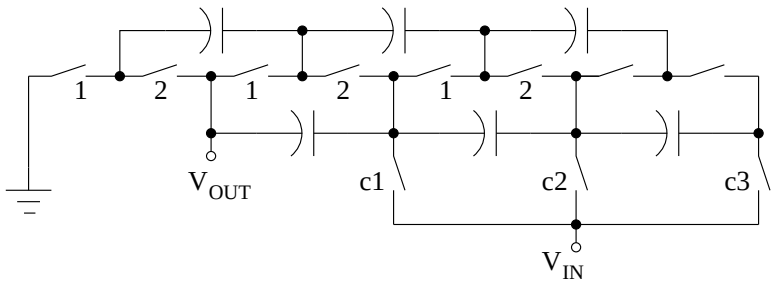


Figure 17: Switched-input regulation ladder-type converter

By switching the input source, a number of conversion ratios can be obtained, yielding an efficient method of voltage regulation. However, if the switching frequency is not modulated appropriately, the output voltage will experience a large step as the input source switches taps. Thus, if output voltage must be regulated within a tight margin, a frequency-modulated control scheme must be used to compensate for the input-switching-induced steps in output voltage.

6 Simulation Results

To verify the algebraic performance calculations for switched-capacitor DC-DC converters derived in the previous sections, simulations in *spectre*^{TM} are performed. In these simulations, only ideal elements were used and parasitics were added explicitly as additional resistors or capacitors.

6.1 Ideal Converter Output Impedance

The first simulation simulates the ideal characteristics of a SC converter, as described in section 2. The 3-to-1 step-down ladder circuit in figure 2 was used. The total capacitor energy storage and total switch V-A product were selected arbitrarily and the individual components were optimized using the methods in section 3. Capacitor C2 was set to 200nF while capacitors C3 and C4 were set to 100nF, proportional to their charge flows. Likewise, switches SW1 and SW2 have a on-state resistance of 50 $m\Omega$ while the other four switches have an on-state resistance of 100 $m\Omega$. The output is modeled with a large capacitance (10 μF) and a current source load. The corresponding output impedance (SSL and FSL) is given by:

$$R_{SSL} = \frac{1}{f_{sw}} \left(\frac{(1/3)^2}{100nF} + frac(1/3)^2 100nF + frac(2/3)^2 200nF \right) = \frac{4.4M\Omega}{f_{sw}} \tag{97}$$

$$R_{FSL} = 2\left(2 \cdot (50m\Omega)(2/3)^2 + 4 \cdot (100m\Omega)(1/3)^2\right) = 178m\Omega \tag{98}$$

Finally, an input voltage of 3 volts was used, yielding a nominal output voltage of 1 volt.

The simulated output impedance was calculated through a time-based simulation where a load current step was applied after the converter reached steady-state. For this converter, a load step of 10 mA was used. The load voltage sag when the converter reached steady-state again was measured and used to calculate the output impedance. The simulated transient appears in figure 18 for a switching frequency of 50 MHz. After repeating the simulation for a range of switching frequencies, the output impedance curve was compared to the calculated results in figure 19. The total calculated SSL and FSL curve was approximated by:

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{99}$$

The simulation results on the SSL and FSL impedance asymptotes match the calculated results very well,

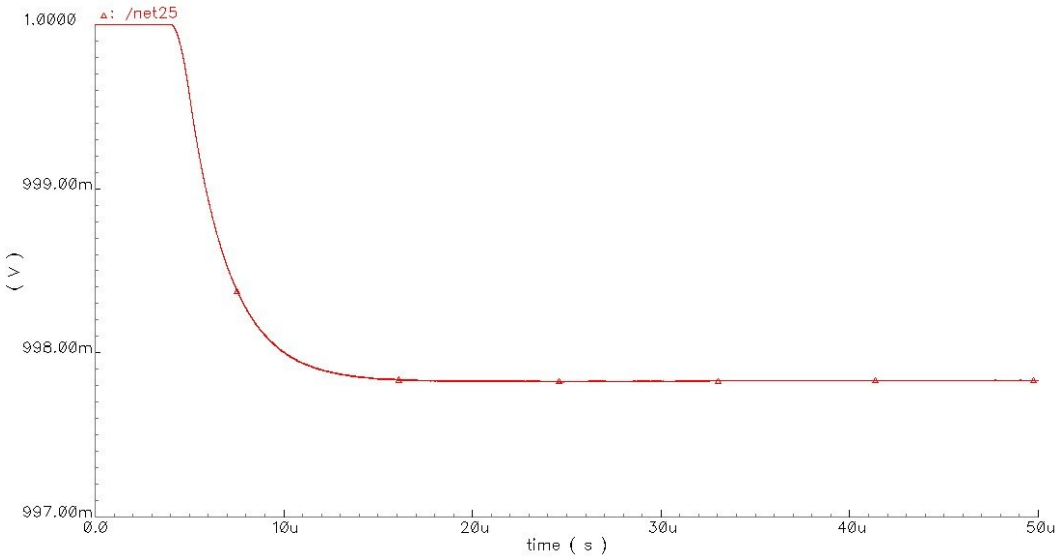


Figure 18: Transient for a 10mA load step ($f_{sw} = 50MHz$)

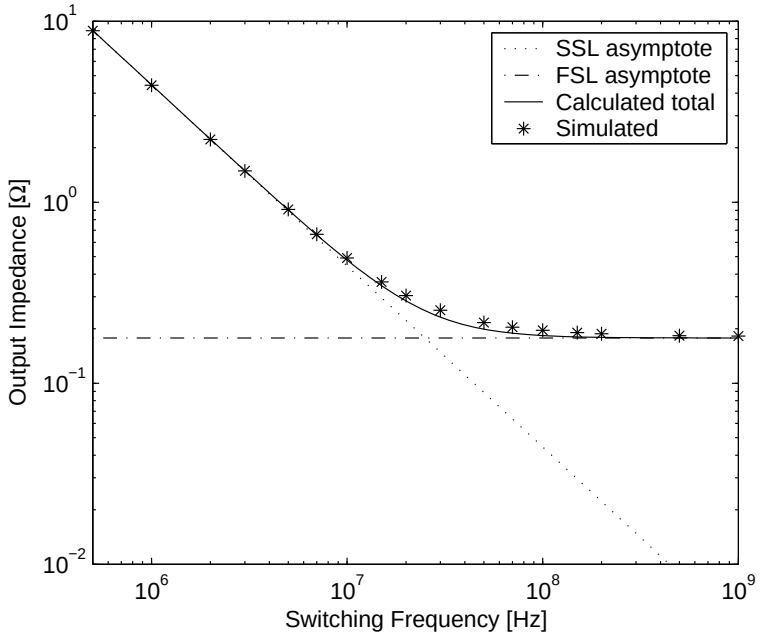


Figure 19: Simulated output impedance vs. switching frequency

demonstrating that the calculations are correct. In the transition between the SSL and FSL, the simulation results do not quite match the approximate transition, as the output impedance does not follow the simple rolloff approximation. Adding the two limits instead of using the relation in equation (99) yields a worse approximation. However, for most practical purposes, the rolloff model provides a sufficient approximation of the output impedance. These results were expected from the calculations and discussion in section 2.

6.2 Gate Drive Performance

The cascode level-shifting gate drive discussed in section 4.2 was simulated to ensure proper level-shifting operation and that the propagation delay was sufficient to operate at high frequencies. This gate drive was used in a high-power 12 volt to 1 volt converter using the Dickson charge pump topology. It was simulated using high-voltage (2.5 volt) transistors in the ST Microelectronics 0.13 μm process. Two turn-on and turn-off transients are shown in figure 20. The gates for only one phase are shown; the other phase looks similar. Sufficient dead-time was given between phases.

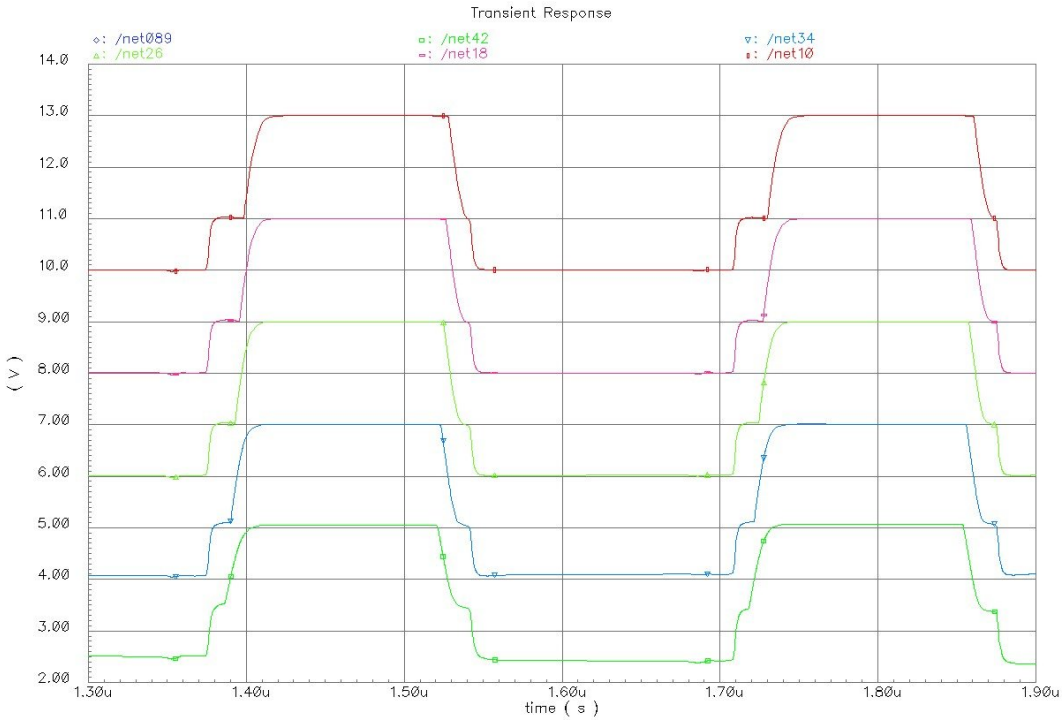


Figure 20: Gate Drive Simulation

The cascode level-shifters work correctly, translating the signal up the entire ladder of transistors. The maximum operation frequency of a SC converter is limited by the dead-time. During each phase transition, one set of transistors must turn off completely, requiring a number of propagation delays. Once all transistors are off, the other set of transistors can turn on, also involving a number of propagation delays as the turn-on signal propagates up the gate drive ladder. This propagation delay, averaged over the 4 delays shown, is 2.89 ns on the rising transition and 1.56 ns on the falling transition per stage. Thus, a converter using this gate drive structure can obtain switching frequencies in the tens of megahertz. Again, it is vital that all transistors in phase 1 turn off before any phase 2 transistors turn on to avoid short-circuit current. Thus, the gate-drive propagation delay is an important consideration in the power limits of a SC converter.

6.3 Parasitic Loss

To simulate the effects of parasitic capacitance to ground, stray capacitors to ground were inserted in the ladder converter simulated in section 6.1 (shown in figure 2). Parasitic capacitors equal to 0.1% of the flying capacitors' values (for discrete applications) were connected between the lower-potential plate of each flying capacitor and ground. Thus, a 200pF capacitor was added for capacitor C2 and a 100pF capacitor was added for C4. Both of these parasitics have a $\Delta v_{c,gnd}$ of 1 volt based on the nominal output voltage of 1 volt. The power loss due to these parasitics is given by:

$$P_{cap,gnd} = f_{sw}\left((100pF)(1V)^2 + (200pF)(1V)^2\right) = 300pW \cdot f_{sw} \tag{100}$$

The equivalent power-loss impedance can be determined (for a 10 mA load):

$$R_{PWR} = P_{cap,gnd}/i_{out}^2 = 3\mu\Omega \cdot f_{sw} \tag{101}$$

The simulation in section 6.1 was performed again, where the output impedance and input power was measured. The simulated power loss due to parasitic capacitance matches the calculated results precisely. From the input power, the power loss impedance (see equation (96)) was calculated. These impedances are plotted in figure 21.

The parasitics start dominating the output impedance approximately at the crossover frequency f_z. This effect of this type of parasitics on the output impedance is impractical to calculate, and is not included in the

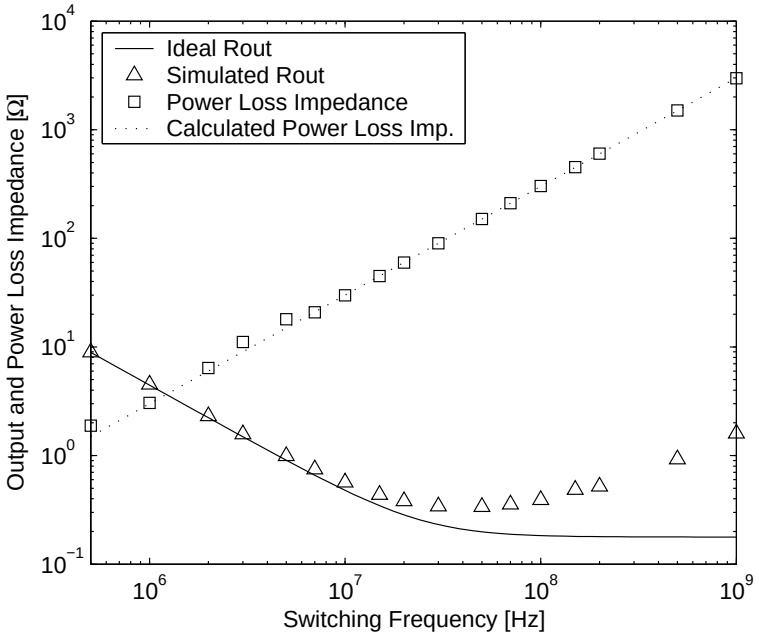


Figure 21: Simulated output impedance with parasitics

mathematical model developed in this work. The simulated parasitic power-loss impedance matches the calculated result (equation (101)) exactly for high frequencies. The parasitic power-loss impedance dominates the actual output impedance at switching frequencies above 1 megahertz at a load current of 10 mA. This equivalent power-loss impedance would decrease for higher load currents as i_{out} increases while $P_{cap,gnd}$ stays constant. In many SC converters, parasitics dominate power loss, and should be considered over output impedance when calculating power efficiency. In addition, when making a converter with integrated switches and/or capacitors, the parasitics must be carefully controlled and minimized whenever possible.

7 Conclusion

Switched-capacitor (SC) power converters can be used for efficient power conversion when inductors cannot be used for size, cost or other reasons. In addition, SC DC-DC converters are superior to inductor-based converters for high-conversion ratios or when the load current can vary over many decades. Analysis methods for SC DC-DC converters have been developed in other works [4, 2], but they have not been completely general. In addition, most of those methods rely on complicated matrix algebra to determine a converter's performance.

Through inspection, a converter's charge multiplier vectors (denoted $\boldsymbol{a_c}$ and $\boldsymbol{a_r}$ for capacitors and switches, respectively) can be determined and define the charge that flows through a component with respect to the output charge flow. This charge multiplier vector is used to derive the primary performance metric for SC converters: their output impedance. The output impedance both defines the output voltage droop for a given output load and the power loss due to conversion inefficiencies. This impedance has two asymptotic limits, the slow switching limit (SSL) and the fast switching limit (FSL). The SSL output impedance is inversely proportional to switching frequency and is capacitor limited. The FSL output impedance occurs when the switch on-state resistance dominates at high switching frequencies, and is independent of switching frequency.

Based on the simple expressions for output impedance, an optimization method was determined for minimizing the output impedance with a constraint on switch size and capacitance. The total energy storage of all capacitors was held constant, as that constraint most accurately reflects physical size and cost. Likewise, the sum of the V-A products of all the converter's switches is held constant. A simple expression for optimal capacitance, switch size and output impedance was determined.

Five popular SC converter topologies were compared in terms of performance given constraints on capacitor energy and switch area, as described previously. Topologies such as the ladder and Dickson charge pump are optimal when switches are the limiting factor. The series-parallel topology is optimal for capacitor-limited applications. The exponential topologies (Fibonacci and doubler) perform reasonably well in both the FSL and SSL comparisons. However, the exponential topologies suffer when implemented, as the switches and capacitors support a wide range of voltages and many of the switches are not DC-referenced.

The ladder topology converter was compared to a standard inductor-based boost converter and a transformer-based converter. The loss due to switch conductance was computed for all three optimized topologies over a range of conversion ratios. For large conversion ratios, the switched-capacitor converter is far superior to the boost converter and equal to the transformer-based converter. However, for conversion ratios less than 2, the boost is superior. Thus, for large conversion ratios, switched-capacitor converters have a distinct advantage over some inductor based converters.

Next, implementation details were discussed, including gate-drive methods and topology modifications for discrete capacitors. A cascode level-shifting gate drive circuit was developed to drive gates of floating transistors efficiently using low-voltage devices. The ladder and Dickson charge pump topologies can be modified to take advantage of ceramic capacitors which achieve a higher energy density at higher voltage ratings. Expressions for power loss due to various circuit parasitics were also derived. This parasitic power loss is mostly proportional to frequency and limits the practical switching frequency of a SC DC-DC converter.

Control methods were discussed to regulate the output voltage of a SC converter. Frequency modulation regulates the output voltage by using the SSL output impedance to dissipate the difference between the nominal and desired output voltages. Although this method is lossy (similar to an LDO), it is effective over a small range of desired output voltages near the nominal output voltage. A hysteresis control method can be used to effectively regulate the switching frequency by switching between two frequency limits based on the output voltage. Second, a method of coarsely but efficiently regulating the output voltage through input or output voltage taps was developed. The combination of the two control methods can be used to create a fully-regulated SC converter.

Finally, the expressions for SC converter performance were verified through simulation. The converter output impedance matched calculated values for both the slow and fast switching limits. In addition, the performance of cascode level-shifting gate drive as simulated and is adequate for switching frequencies into the tens of megahertz. Finally, the effects of parasitic elements in a SC converter was simulated. It is important that all parasitics and short-circuit current be minimized for correct operation.

Simple methods have been developed to enable thorough analysis of any given switched-capacitor con-

verter. The practical aspects of a number of converter topologies hve been discussed. These analysis and optimization methods can be used to design a generation of high-performance switched-capacitor converters and extend their use into applications where they have not been utilized to date.

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