A 2.4GHz, 20dBm Class-D PA with Single-Bit Digital Polar Modulation in 90nm CMOS

Jason T. Stauth and Seth R. Sanders

University of California, Berkeley, CA, 94720, USA

Abstract — **Polar transmitters are a promising alternative to traditional Cartesian architectures in terms of flexibility and power efficiency. Such systems are often difficult to implement due to wideband amplitude and phase signals and may require predistortion to meet EVM and spectral requirements. This work demonstrates a highly-linear digital-polar system implemented in 90nm CMOS. The amplitude is controlled with pulse-density modulation of the RF carrier. Phase information is provided with the RF clock. The class-D PA achieves peak efficiency of 38.5% at 2.4GHz, including power of the PA drivers and insertion loss of the bandpass filter. The system does not require predistortion, and achieves rms-EVM levels of 1.8-2.1% for π/4DQPSK and 8DPSK test vectors. The spectral mask for Bluetooth 2.1+EDR is satisfied under normal operating conditions.**

I. Introduction

Single-chip integration for low-power portable wireless systems is highly desirable to drive lower costs and smaller package footprints. In addition, research directions in cognitive and software-defined radio seek flexible architectures that can operate at multiple carrier frequencies and with different standards. This work presents a promising direction in both the system architecture and circuit implementation that may improve both the flexibility and integration level of the radio transmitter.

Polar transmitter architectures have gained interest in recent years due to improvements in flexibility and efficiency over traditional Cartesian architectures [1, 2]. In the Polar example, the complex RF signal is represented with amplitude and phase components instead of traditional I and Q vectors. This allows the power amplifier (PA) to operate with drain modulation, envelope restoration (ER), or envelope tracking (ET) modes [1-4]. If the power supply of the PA is modulated by an efficient DC-DC or hybrid switching-linear amplifier, the average efficiency of the system can be improved significantly [1, 4]. In true polar modulation there is no need for quadrature upconversion in the mixing stage. This can reduce passive components and make it easier to adjust the carrier frequency of the transmitter. Common difficulties in polar systems result from the fact that amplitude and phase are not bandlimited as with Cartesian I and Q signals. This drives the need for wideband amplitude and phase modulators to meet spectral masks and achieve low error-vector magnitude (EVM) levels. Also, supply modulated and envelope tracking PAs may experience significant AM-AM and AM-PM distortion from the polar process. Many published solutions require complex predistortion algorithms to meet linearity requirements [1, 2].

This work presents a digital polar modulation transmitter with a class-D power amplifier. Instead of modulating the supply voltage, the amplitude is controlled with pulse-density modulation of the RF carrier. To achieve high resolution and reduce out-of-band noise, we use two stages of noise shaping. The first stage uses multi-bit ΔΣ modulation operating at 100MHz (up to 100 times oversampling). The second stage is a pre-programmed 1-bit pulse-density modulation (PDM) scheme operating at the RF carrier frequency.

The second-stage modulator and class-D PA are implemented in 90nm CMOS. To achieve higher output power (up to 20dBm) with standard oxide devices, the PA uses a cascoded CMOS output stage. A matching network and bandpass filter are used to help attenuate out-of-band noise. The class-D PA achieves efficiency of 38.5% at 2.4GHz including all driver power and insertion loss of the filter.

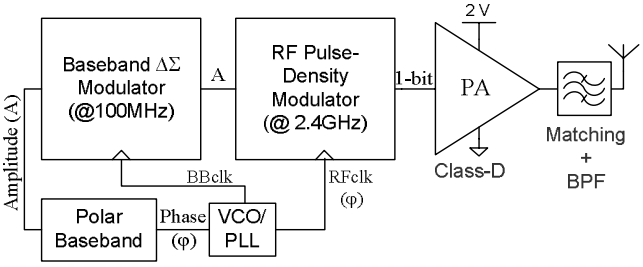


Fig. 1 Digital polar modulation architecture

II. Architecture

The architecture, shown in Fig. 1, uses a polar digital baseband to control the amplitude and phase components of the transmitted RF signal. The amplitude information passes to the first stage ΔΣ modulator. The ΔΣ stage converts the signal to an oversampled representation with 10 quantization levels and a polarity bit. The polarity bit is used to smooth discontinuities in the phase signal when the amplitude is near zero. This is done by implementing phase inversions in the amplitude path instead of the phase path which significantly reduces the bandwidth of the *RFclk* signal. This also improves the linearity of the ΔΣ process when the amplitude is near zero by preventing saturation of the multi-bit output.

The ΔΣ modulator controls a programmed RF pulse-density modulator that converts the signal to 1-bit quantization operating at 2.4GHz. The ΔΣ and PDM blocks are synchronized with clock signals that contain the polar phase information. In the case of the PDM stage, the clock signal operates at the RF carrier frequency of 2.4GHz. In a fully integrated implementation, the polar baseband would control a VCO to regulate the baseband and RF clock signals. In our implementation the RF clock with phase information is generated off chip with a Labview PXI system.

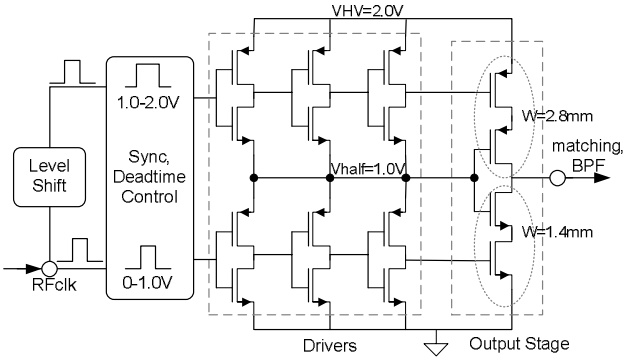


Fig. 2 CMOS Class-D cascode PA

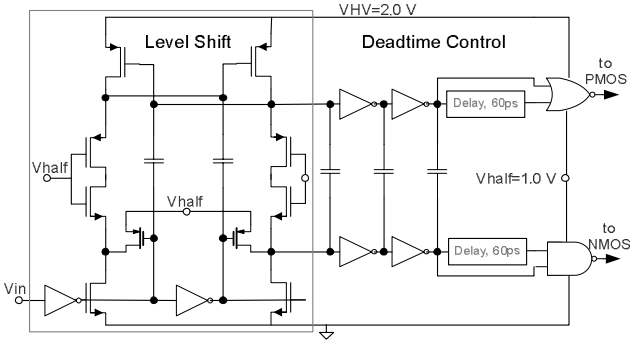


Fig. 3 Level shift and deadtime control

III. Class-D PA

Shown in fig. 2, the class-D PA operates with both NMOS and PMOS complementary devices. With PMOS f_t exceeding 40GHz in the 90nm process, the P-channel device does not significantly reduce efficiency. To achieve higher power, the output stage is cascoded. The PA provides power gain and interfaces with a matching network and high-order bandpass filter to attenuate out-of-band quantization noise. The level shift circuit, shown in fig. 3, interfaces the 1-bit polar signal to the cascode output stage. The PA normally operates with maximum power rail *VHV=2.0V* and a mid power rail *Vhalf=1.0V*. This limits the maximum oxide stress to 1.0V in normal operation. The deadtime circuit prevents shoot-through current and synchronizes the output stage voltage waveforms. A nominal 60ps deadtime optimizes power efficiency while providing a reasonable buffer for process and temperature variation. A 100pF on-chip bypass capacitor supplies high-frequency current from the *VHV* node.

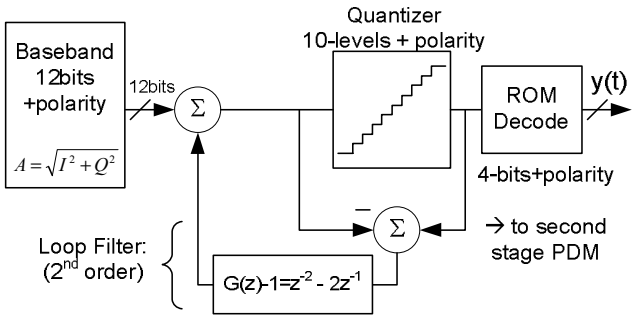


Fig. 4 Error-feedback digital ΔΣ modulator

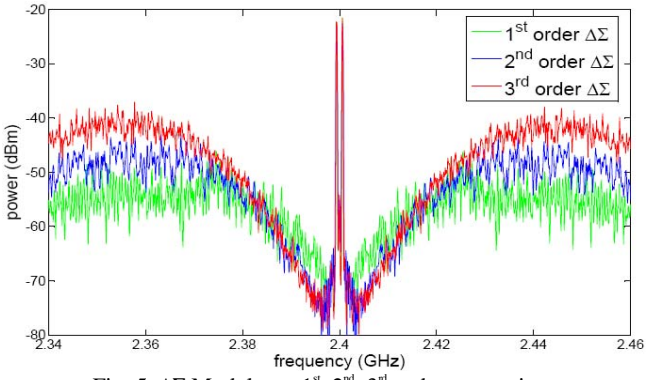


Fig. 5 ΔΣ Modulator: 1st, 2nd, 3rd-order comparison

IV. ΔΣ Modulator

The ΔΣ modulator is implemented with a digital error-feedback structure, as shown in fig. 4 [5]. In this example, the quantizer extracts 10 levels and the polarity of the 12-bit representation. A ROM decoder maps the bi-polar 10-level quantization to 4-bits with polarity for the next-stage PDM block. The system is clocked at the baseband frequency of 100MHz, so peaks in the noise spectrum occur roughly 50MHz centered at the carrier frequency.

Fig. 5 shows the simulated frequency response of the system with various loop filters for a suppressed carrier AM signal. The 3rd order system has the lowest noise at the center frequency, but highest peak out-of-band noise. The first-order system has lower peak out-of-band noise, but may have tones in the output spectrum for certain input signals [5]. A second-order filter achieves both favorable noise-shaping and reduced possibility of tones in the output spectrum. The second-order filter was used in the final design.

V. Pulse-Density Modulator

The pulse-density modulator (PDM) block converts the output of the ΔΣ block to a 1-bit representation. The ΔΣ output is sampled with a synchronous 100MHz clock and then re-synchronized to a set of shift registers operating at 2.4GHz (*RFclk* signal with phase information). The shift registers generate a PDM waveform from pre-programmed binary codes stored in an on-chip ROM. The codes represent bit sequences corresponding to 10-level amplitude quantization. Tones from the programmed bit sequences occur far from the

carrier frequency to maximize filter attenuation. The clock recovery circuit inverts the phase of the clock depending on the polarity bit. This allows polarity information to be synchronized with the amplitude path, eliminating wideband phase inversions in the phase path. The PDM generation block mixes the PDM signal from the shift-registers with the RF clock. The RF clock contains phase information and the PDM signal contains amplitude information. The result is a polar modulated 1-bit output that is provided to the class-D PA.

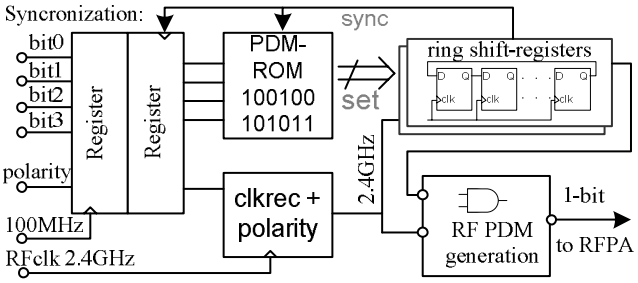


Fig. 6 Pulse-density modulator block

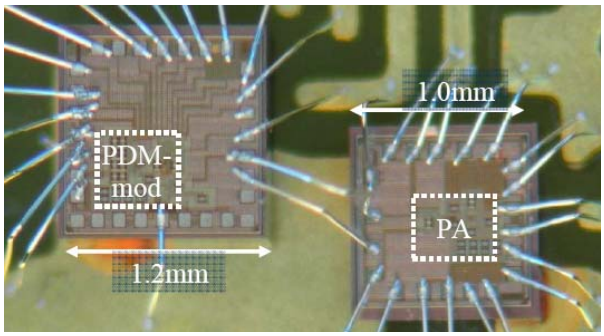


Fig. 7 Die Photo

VI. Experimental Results

The system is implemented with two test chips in 90nm CMOS. A first chip contains the class-D PA and drivers (active area 0.15mm^2). A second chip contains the PDM structure, synchronization, clock recovery and ROM (active area 0.2mm^2). A die photo is shown in fig. 7. The baseband and ΔΣ modulator are implemented in an FPGA. The system is tested with a Labview PXI setup with RF upconverter and downconverter. The labview system and FPGA use a synchronous clock to perform time-alignment of the amplitude and phase signals. The output filter is implemented off-chip and consists of a traditional L-matching network and an additional surface-mount bandpass filter component. The bandpass filter is a Johanson 2450BP41D100B component for the 2.45GHz band with 1.3dB maximum insertion loss.

Fig. 8 shows the total output power and efficiency of the class-D PA across supply voltage. Here, efficiency includes power of the PA drivers and loss in the matching network, but does not include insertion loss of the bandpass filter. The peak output power of 20dBm occurs for the maximum supply voltage of 2.4V (oxide stress of 1.2V). The peak efficiency of 40.7% occurs for a supply voltage of 2.0V. With the bandpass filter included, peak efficiency was measured at 38.5%. Fig. 9 shows linearity and efficiency at each of the 10-levels of amplitude quantization. Linearity for the PA is high with pulse-density modulation. Importantly, efficiency stays higher at lower power levels than with typical class A/AB power amplifiers. Efficiency of the PA, including driver power, stays above 25% for 10dB power backoff.

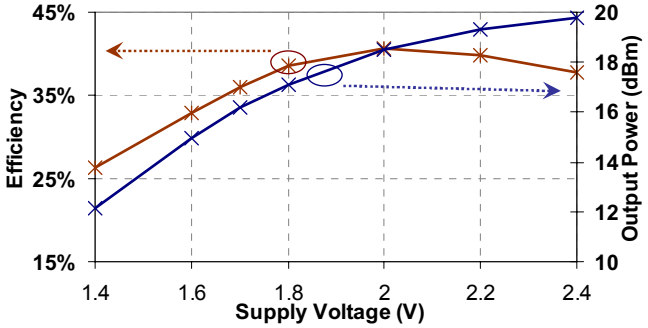


Fig. 8 Efficiency and output power vs supply voltage

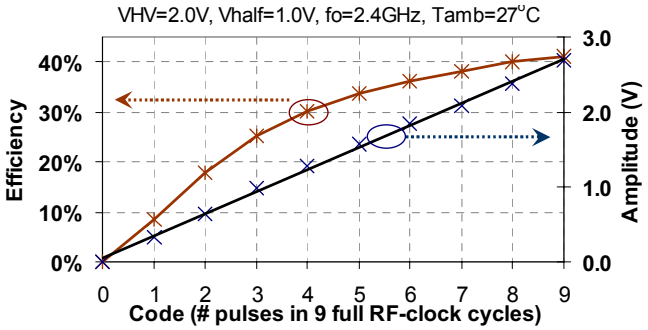
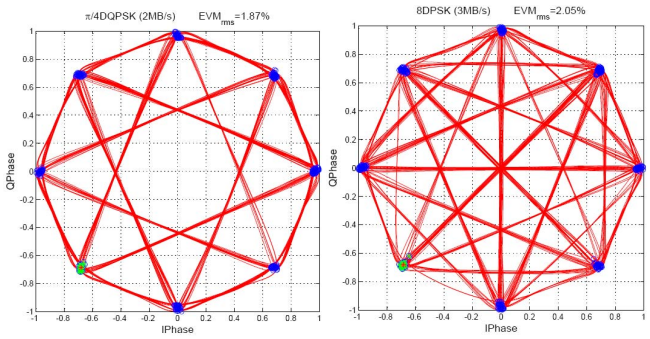


Fig. 9 Efficiency and linearity vs pulse-density

The average efficiency of the system is further improved with a current recycling scheme. Since the *Vhalf* node in the PA operates at 1.0V, this node can be shared with the 1.0V V_{DD} node. This allows excess current from driving the PMOS power device in the PA to be used to power the remaining 1.0V circuitry. At 2.4GHz this reduces the current drawn from the 1.0V supply from 11.7mA to 3.7mA. The current recycling scheme allows the entire system to operate with 30% average efficiency for π/4DQPSK and 8DPSK modulated signals with approximately 3dB PAPR.

Low digital processing power and high average efficiency make this scheme amenable to low-power portable wireless standards, such as Bluetooth. Comparable work published in the literature achieves higher spectral fidelity at the tradeoff of significantly higher power consumption. [6] demonstrates a system with ΔΣ DACs operating at 5.4GHz that meets cellular coexistence requirements for 802.11b/g and 802.16e. Reported current consumption is 83mA from a 1.2V supply for the digital block. RF current consumption is 128mA for rms output power of 2.6dBm. Our solution requires between 2-5mW for the digital PDM block and roughly 55mW RF power for 12-14dBm rms output power level.



a.) π/4DQPSK (2MBPS) b.) 8DPSK (3MBPS)

Fig. 10 Measured constellation diagrams

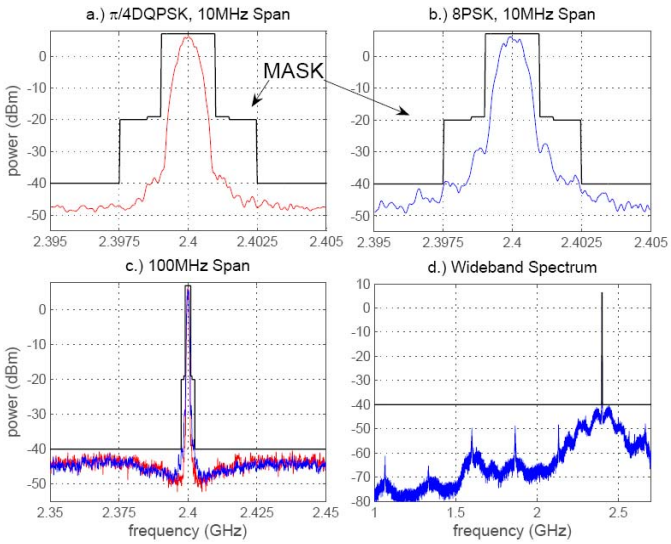


Fig. 11 Transmitter output spectrum, 100kHz RBW

Fig. 10 shows the measured constellation diagram for π/4DQPSK and 8DPSK test vectors. These test signals meet the requirements of the Bluetooth 2.1+EDR standard for the 2MBPS and 3MBPS datarates [7]. Measured EVM for π/4DQPSK is $EVM_{rms} = 1.8\%$ and $EVM_{peak} = 2.8\%$, and for 8DPSK, $EVM_{rms} = 2.1\%$ and $EVM_{peak} = 2.9\%$. As seen for the 8DPSK data in Fig. 10-b, the transmitter is capable of generating constellation trajectories that pass through the origin (infinite peak-minimum ratio). The system remains linear near zero amplitude, minimizing low amplitude distortion by synchronizing polarity shifts with the digital polarity bit in the amplitude path. This significantly reduces the bandwidth requirements of the phase modulator and improves performance for high PAPR signals.

Quantization noise of the digital modulator is a limiting factor for spectral performance. Fig. 11a-d shows that the nearband spectral requirements for Bluetooth 2.1+EDR are satisfied for both π/4DQPSK and 8DPSK test signals. Average power levels at the spectrum analyzer are between 11-14dBm. The wideband spectral mask is satisfied due to the addition of the bandpass filter at the output. However, it should be noted that in peak-hold mode, which is required for the Bluetooth standard, there is little margin for the -40dBm power limit (100kHz RBW). Shown in fig. 11-c, the lowest margin occurs near peaks in the quantization noise spectrum 50MHz from the center frequency. Low margin in the spectral mask could make the system susceptible to load pull, power supply variation, or other scenarios which cause wideband noise levels to increase. This can be improved by operating the ΔΣ process at higher clock frequencies, or reducing the transmitter power level. In a fully-integrated version, it may be practical to operate the ΔΣ modulator at 250MHz or more, reducing the peak noise by 3-10dB, depending on the filter component. Due to limited margin in meeting the spectral-mask, we do not present this as a fully-functional Bluetooth transmitter, but rather a demonstration of a new and interesting topology worthy of further investigation. The high efficiency and excellent linearity show that this is a promising alternative to traditional Cartesian and polar transmitters.

VII. Conclusion

We have presented a new architecture for digital polar modulation using a class-D PA. The amplitude is controlled with pulse-density modulation through baseband ΔΣ modulation and an RF pulse-density modulation circuit. The PA achieves peak efficiency of 38.5% at 2.4GHz, including driver power and insertion loss of the filter. The system achieves high linearity across the full power range, achieving rms EVM of approximately 2%. The spectral masks for the Bluetooth 2.1+EDR standard are met for both 8DPSK and π/4DQPSK test vectors. Limited margin near peaks in the quantization noise spectrum motivates additional research to further reduce out-of-band noise levels.

References

[1] F. Wang, D. Kimball, D. Y. Lie, P. Asbeck, and L. E. Larson, "A Monolithic High-Efficiency 2.4GHz 20dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier," *IEEE Journal of Solid State Circuits*, vol. 42, pp. 1271-1281, June 2007.

[2] P. Reynaert and M. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE Journal of Solid State Circuits*, vol. 40, pp. 2598-2608, Dec. 2005.

[3] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power Amplifiers and Transmitters for RF and Microwave," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, March 2002.

[4] J. T. Stauth and S. R. Sanders, "Optimum Biasing for Parallel Hybrid Switching-Linear Regulators." *IEEE Transactions on Power Electronics*, vol. 22, pp. 1978-1985, Sept. 2007.

[5] S. R. Norsworthy, R. Schreier, G. C. Temes, and IEEE Circuits and Systems Society., *Delta-Sigma data converters : theory, design, and simulation*. New York: IEEE Press, 1996.

[6] A. Pozsgay, T. Zounes, R. Hossain, M. Boulemnakher, V. Knopik, and S. Grange, "A Fully Digital 65nm CMOS Transmitter for the 2.4-to-2.7GHz WiFi/WiMAX Bands using 5.4GHz DS RF DACs," *IEEE International Solid State Circuits Conference (ISSCC) Dig. Tech. Papers*, vol. 51, pp. 360-361, Feb. 2008.

[7] Bluetooth_Special_Interests_Group_(SIG), "Bluetooth technical specifications," in www.bluetooth.org, 2008.