Efficiency Optimization for Dynamic Supply Modulation of RF Power Amplifiers

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Research Project

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Approval for the Report and Comprehensive Examination

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Chapter 1

Introduction and Motivation

The IC industry has experienced an exponential growth in the past decades. At the center of this growth is the emergence of portable electronics, such as laptops, cell phones, and smart phones. In order to allow for convenient communication between portable devices, many different wireless communication schemes, along with different modulation schemes have been invented.

One important block in wireless communication is the RF Power Amplifier (PA). The requirement on RF PAs is rather stringent in many different areas, such as high output power level and high linearity. These specifications are met often at the expense of power consumption. The goal of efficiency improvement in RF PAs has been explored over the years. A number of techniques, such as the polar architecture [1], the envelope tracking architecture [2], digital PA [3], Doherty [4], have been invented.

Both the polar architecture and the envelope tracking architecture belong to the class of dynamic supply modulation techniques. In this approach, the power supply voltage of the PA is varied in synchronization with the envelope of the RF input voltage. In essence, when the envelope of the RF signal is low, the supply voltage is also reduced to minimize power consumption. Dynamic supply modulation technique therefore requires a highly power efficient, wide bandwidth, and wide swing dynamic supply regulator.

The goal of this research is to explore techniques to realize highly efficient dynamic supply regulators. There are a number of supply regulator architectures, such as the wideband switching regulator [5], the parallel hybrid linear switching regulator [6-8] and the series hybrid linear switching regulator [9]. In this work, the parallel hybrid linear switching regulator is being investigated. In this architecture, a linear regulator is placed in parallel with a switching regulator to obtain both the wide bandwidth tracking ability of the linear regulator and the high efficiency of the switching regulator.

Chapter 2 discusses background information regarding dynamic supply modulated PA architectures and dynamic supply regulator architectures. Previous work on parallel hybrid linear switching regulators is also discussed. Chapter 3 discusses the theory of optimizing the parallel hybrid linear switching regulator. Simulation results are provided. Furthermore, an optimizing circuit block diagram is proposed. Chapter 4 discusses the design of an envelope amplifier. A method of controlling crossover current is proposed and designed.

Chapter 2

Background

This chapter gives a brief background on transmitter architectures and dynamic supply regulator architectures. Next, the chapter will discuss previous work done in the area of parallel hybrid linear switching regulator.

2.1 Transmitter Architectures

Conventional Transmitter Architecture

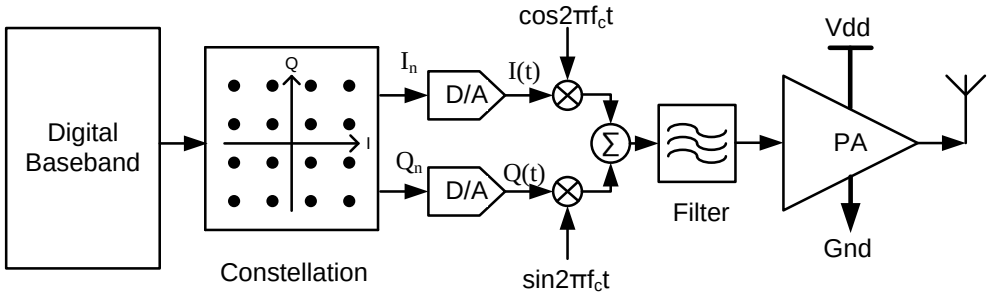

Figure 2.1 Conventional Transmitter Architecture

Figure 2.1 contains a block diagram for a conventional RF transmitter. The digital output from the baseband is mapped onto a constellation plot (16 QAM in this case). The bits are converted to in-phase, I, and quadrature, Q components. Components, I and Q, are separately upconverted by local oscillators to the desired RF carrier frequency. They are further summed

together before being applied to the input port of the RF PA. The job of the PA is to amplify the input RF signal to the desired output power level required for adequate radio communication. The power supply voltage of the RF PA is a nominally constant value, Vdd. In the cases of linear PAs, such as Class-A, AB, and B, the efficiency of the PA drops significantly as the output voltage swing falls below the compression point. Figure 2.2 is a plot of maximum ideal efficiency of Class A and Class B PAs as a function of output voltage swing. The following discussion considers two transmitter architectures that are designed to improve efficiency as the output voltage swing of the RF PAs is reduced.

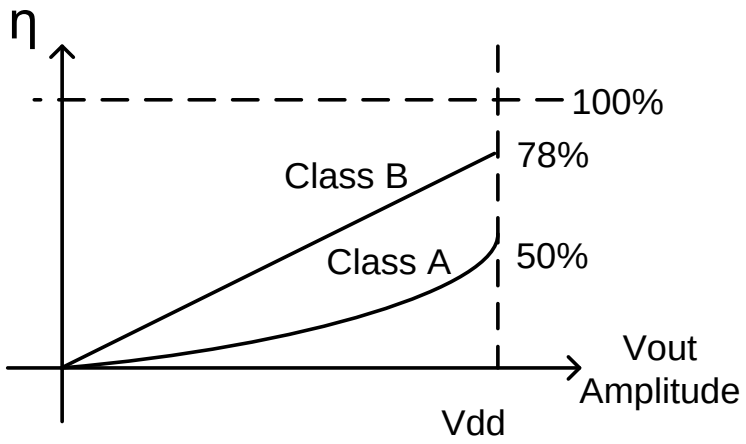

Figure 2.2 Ideal Efficiency of Class A, B PAs versus Output Voltage Amplitude

Envelope Tracking Architecture

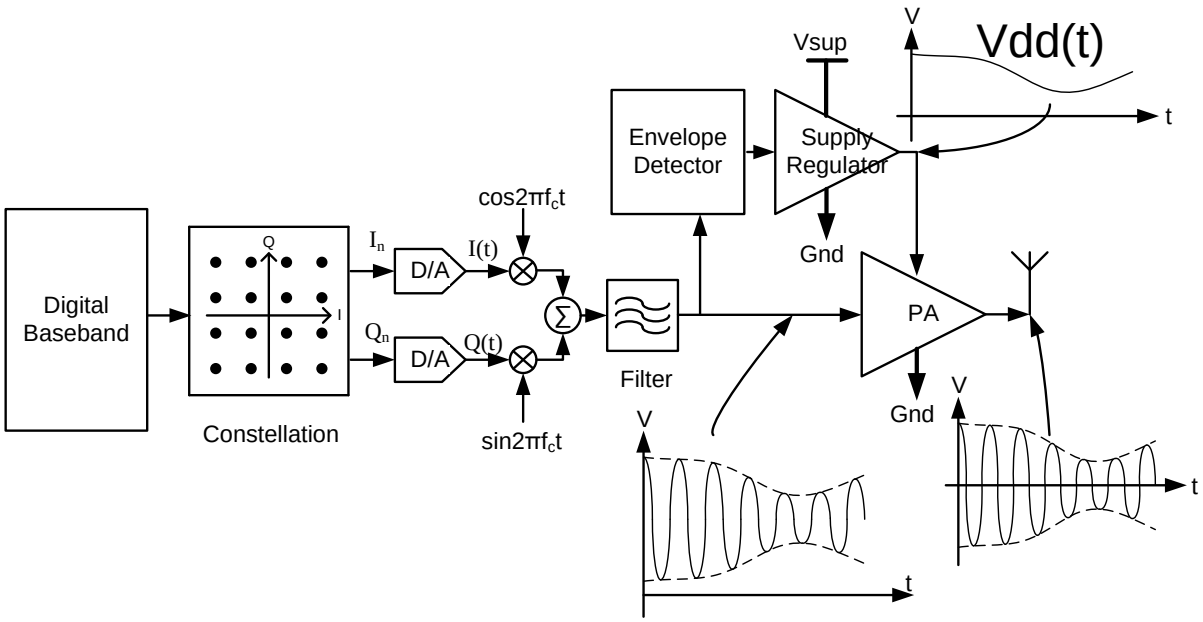

Figure 2.3 Envelope Tracking Transmitter Architecture

Figure 2.3 shows a block diagram for the Envelope Tracking Architecture. This architecture is almost identical to the previous transmitter architecture. The main difference is that the envelope of the RF input to the PA is extracted by the Envelope Detector. The envelope is amplified by the Supply Regulator to dynamically change the supply voltage, Vdd(t) of the RF PA. When the output amplitude level is low, the supply voltage will drop synchronously with the envelope signal. This will allow the PA to operate very close to its compression point achieving high efficiency at all output voltage swings. Recent work in envelope tracking can be found in references [10-12].

Polar Architecture

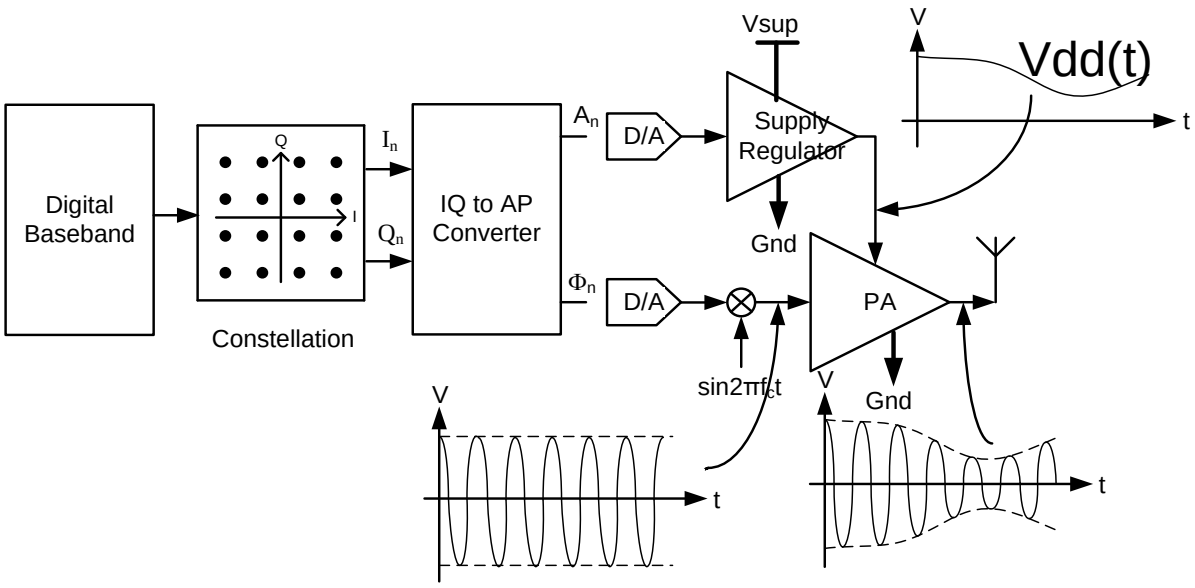

Figure 2.4 Polar Transmitter Architecture

Figure 2.4 shows a block diagram for the Polar Transmitter Architecture. In-phase (I) and quadrature (Q) components are converted to Amplitude, A, and Phase, Φ components. The input to the PA only contains phase information. The PAs used here are usually nonlinear PAs such as Class E and F. Nonlinear PAs are highly efficient but can only provide phase information. The supply regulator replicates amplitude information to the supply of the PA. The supply regulator directly modulates the amplitude of the PA output. Hence, the output signal will contain both amplitude and phase information. The main problem with this architecture is that without linearity enhancement techniques the overall architecture will suffer from poor linearity resulting in poor transmission performance. Recent work in polar architecture can be found in references [13-15].

2.2 Dynamic Supply Regulator Architectures

The efficiency of dynamic supply regulators is central to the overall efficiency of the RF PA. Similarly to the PA, a dynamic supply regulator is designed to handle maximum output power. However, most of the time, supply regulator output power is significantly less than the designed maximum output power. Hence designing a dynamic supply regulator that is power efficient across its output power range and its output voltage range is very important. Furthermore, the supply regulator needs to track the envelope signal of the RF input. Figure 2.5 shows a typical frequency spectrum of sample 802.11g in-phase and envelope signals [20]. The spectrum contains a high peak from DC to several kHz.

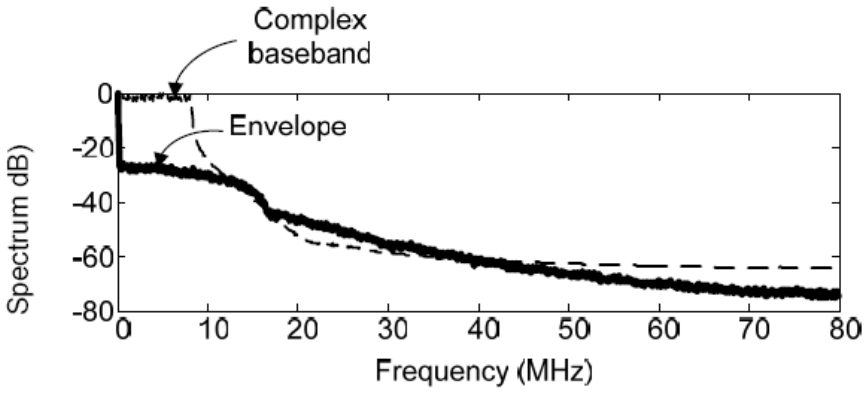

Figure 2.5: Complex Baseband and Envelope Spectrum of sample 802.11g waveform [20]

Wideband Switching Regulator

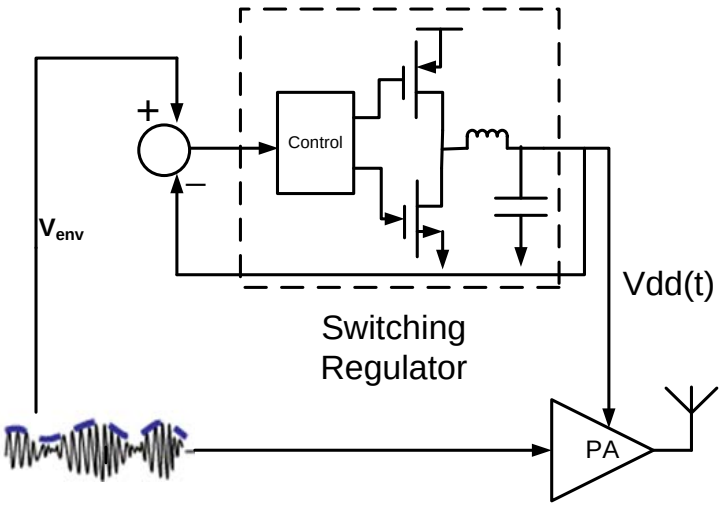

Figure 2.6 Wideband Switching Regulator

Figure 2.6 is a block diagram of a wideband switching supply regulator. Two switches gated in complementary pattern are modulated with a time-varying duty cycle. The output is filtered out by an LC network, creating a smooth, 20MHz bandwidth output signal. In theory, switching regulators can achieve very high efficiency. In order to track signals of bandwidth 20MHz, the loop bandwidth is around 200MHz. This introduces challenges in stabilizing the loop. One recent work in reference [16] uses open-loop control of switching regulator. However, switching frequency is still around 200MHz causing the efficiency to be low. Problems such as parameter variations are part of the challenges in designing open-loop control of switching regulator.

Series Hybrid Linear Switching Regulator

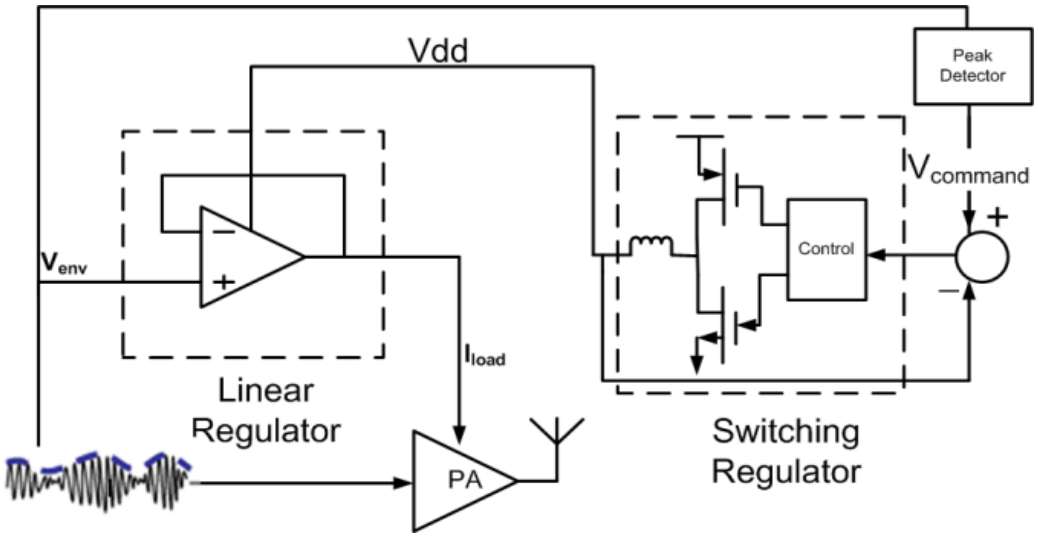

Figure 2.7 Series Hybrid Linear Switching Regulator

Figure 2.7 shows a block diagram of a series hybrid linear switching regulator. The linear regulator is the primary regulator. It replicates the envelope voltage to the supply of the PA. The peak detector tracks peaks of the envelope voltage. The purpose of the switching regulator is to replicate the peaks of the envelope of the RF input. Reference [9] presents an example of the series hybrid. The main issue with the series hybrid regulator is that the efficiency is poor when the peak voltages of the envelope are high creating a large voltage drop in the linear regulator.

Parallel Hybrid Linear Switching Regulator

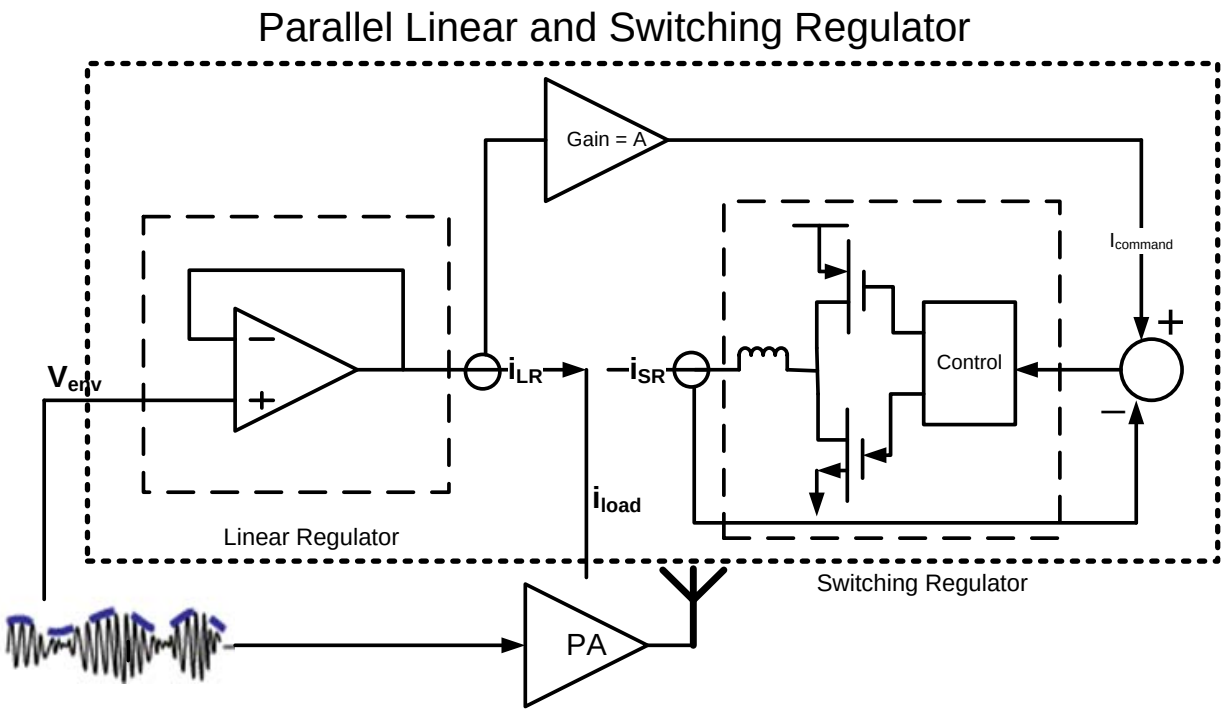

Figure 2.8 Parallel Hybrid Linear Switching Regulator

Figure 2.8 shows a block diagram of a parallel hybrid linear switching regulator. The linear regulator acts as a voltage regulator which ensures the supply voltage of the PA tracks the envelope voltage, V_{env}. The switching regulator acts as a current source. The low frequency output current of the linear regulator is measured, amplified and fed to the input of the switching regulator in conventional designs [17-18]. The switching regulator provides the low frequency current component of the envelope signal. The linear regulator provides the high frequency portion of the envelope signal. The parallel hybrid trades off the advantage of wide bandwidth of the linear regulators with high efficiency of switching regulators. Recent works can be found in references [17-19].

2.3 Previous Work on Parallel Hybrid Linear Switching Regulator

Figure 2.9 shows a simplified model of a parallel hybrid linear switching regulator. The PA supply load is initially modeled as a known resistor. Signal v_{load} is the desired supply voltage of the PA which is directly related to the envelope voltage. The switching regulator is modeled as a 100% efficient current source. This means whatever power the switching regulator provides, the same power goes into the supply of the switching regulator. In addition, the switching regulator only provides a constant unipolar current. The linear regulator is modeled as a sourcing current source and a sinking current source.

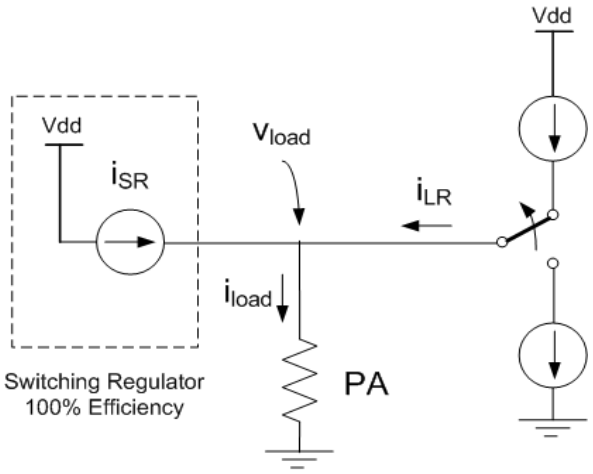

Figure 2.9 Parallel Hybrid Linear Switching Regulator Modeling

In the work done by J. Stauth [19], overall hybrid regulator efficiency is computed for simple v_{load} waveforms as a function of the DC switching regulator current. Previous published designs [17-18] assumed that the switching regulator should provide the dc component and some of the low bandwidth component of i_{load}. In reference [19], the highest efficiency of the hybrid

regulator is achieved at a constant switching regulator current that is not the average of i_{load}. This contradicts the assumption that the switching regulator should provide the low frequency component of the load current for maximum efficiency. The efficiency for real envelope signals such as CDMA and OFDM is measured as a function of the DC switching regulator current [19]. It is shown experimentally that at the highest overall efficiency, the switching regulator does not provide average i_{load} [19]. Figure 2.10 shows the measured efficiency versus average output power for IS-95 code-division multiple-access (CDMA) and 802.11a envelope waveforms [19]. The dashed line is the efficiency when the switching regulator current, i_{SR} is equal to the average of load current, i_{dc}. The gray solid line is the efficiency when i_{SR} is equal to the optimal switching regulator current, i_{SR}* for 802.11a envelope waveforms. The optimal current, i_{SR}* was determined empirically. One can observe large efficiency improvement especially in the range when the average output power is low.

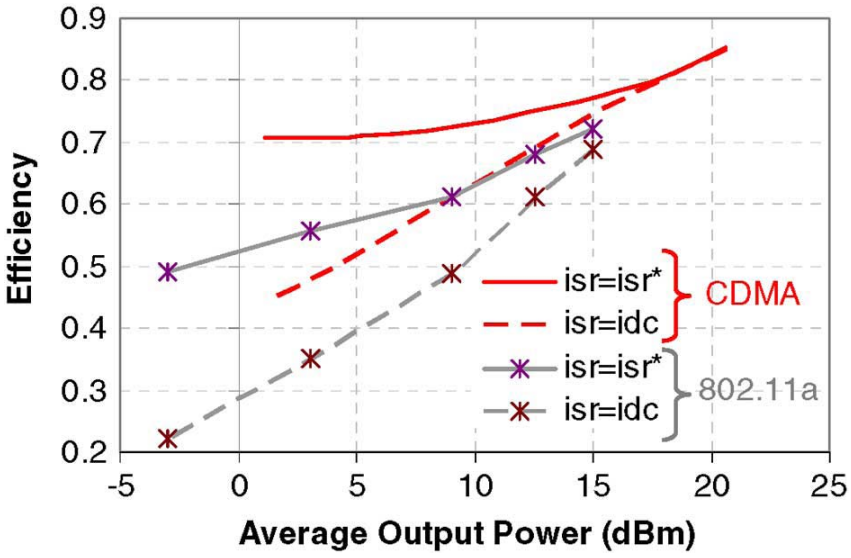

Figure 2.10 Measured Efficiency versus Average Output Power for IS-95 CDMA and 802.11a [19]

Chapter 3

Efficiency Optimization of Parallel Hybrid Linear Switching Regulator

3.1 Mathematical Theory

Key questions addressed in this research are: why is the optimal switching regulator current, i_{SR} not equal to average load current, i_{load}; and how do we compute optimal switching regulator current, i_{SR}^{*} for complicated envelope signals. Figure 3.1 shows a simplified model of the parallel hybrid regulator. The PA is modeled as a black box load, where load voltage, v_{load} and load current, i_{load} can take on any relationship. The switching regulator current is denoted as i_{SR} and the linear regulator current is denoted as i_{LR}. The supply voltage of the linear regulator is denoted as Vdd. When the linear regulator is sourcing current, there is a voltage drop of Vdd – v_{load}. When the linear regulator is sinking current, there is a voltage drop of v_{load}.

Figure 3.2 shows a time domain sample switching regulator current i_{SR}, load current i_{load}, and linear regulator current i_{LR}. The waveforms are restricted to a time window of duration T. Since currents into a node sum to zero, linear regulator current i_{LR} is equal to $i_{load} - i_{SR}$. Since the bandwidth of the switching regulator is small, i_{SR} can be assumed to be a constant value for a time window of duration T. Hence $i_{SR} = I_{SR}$. Whenever i_{load} is greater than I_{SR}, i_{LR} is greater than

0, hence sourcing current. There is an associated voltage drop of Vdd – v_{load}. Whenever i_{load} is less than I_{SR}, i_{LR} is less than 0, hence sinking current. The associated voltage drop is v_{load}.

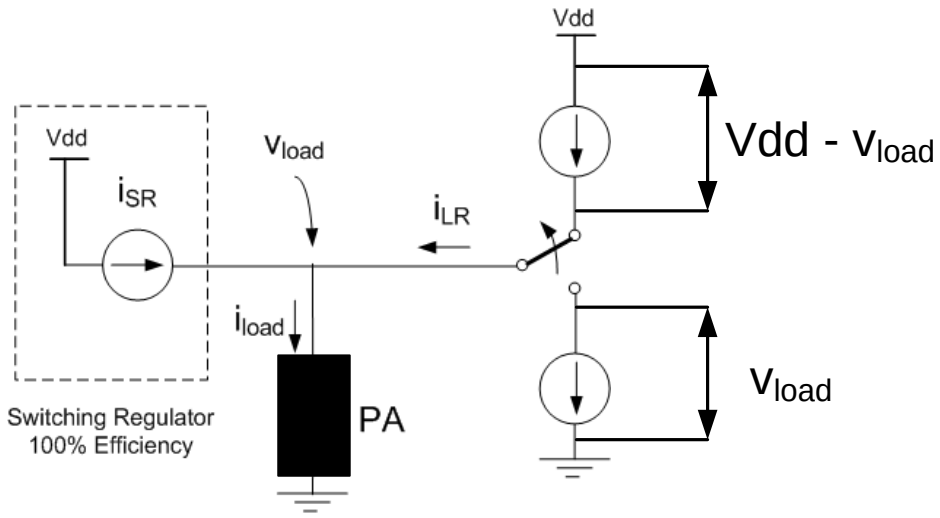

Figure 3.1 Modeling of Parallel Linear Switching Regulator

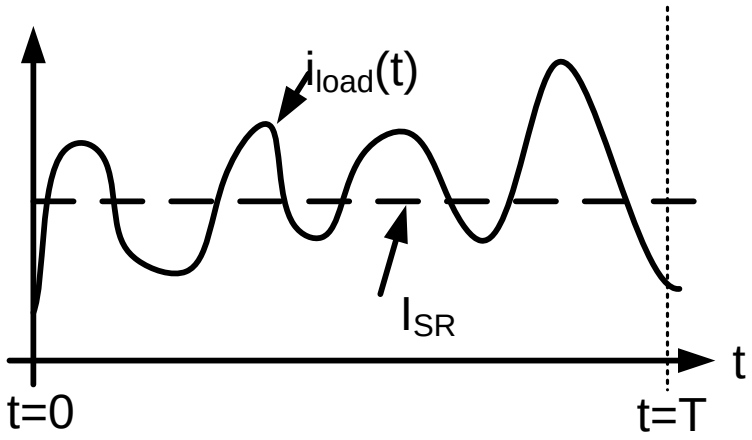

Figure 3.2 Time Doman waveforms of i_{load}, and I_{SR}

Equation (1) is an expression of efficiency, η, in terms of v_{load}, i_{load}, i_{LR}, and Vdd. The numerator is the output energy. The first term in the denominator is the energy drawn by the linear regulator. Note that it draws current from the supply only when the linear regulator current, i_{LR} is greater than 0. Hence i_{LR} is integrated over the time when $i_{LR} > 0$. The second term in the denominator is the energy drawn by the switching regulator. If limits in the integral are not specified, it is assumed that limits of integration are from t = 0 to t = T.

$$\eta = \frac{\int v_{load} \cdot i_{load}\, dt}{Vdd \int_{t:i_{LR}>0} i_{LR}\, dt + \int v_{load} \cdot I_{SR}\, dt} \tag{1}$$

Efficiency, η, is a function of the switching regulator current, I_{SR}.

The objective is to find the optimal I_{SR}* that maximizes η.

$$I_{SR}^{*} = \text{argmax}_{I_{SR} \geq 0}\{\eta(I_{SR})\} = \text{argmax}_{I_{SR} \geq 0}\left(\frac{\int v_{load} \cdot i_{load}\, dt}{Vdd \int_{t:i_{LR}>0} i_{LR}\, dt + \int v_{load} \cdot I_{SR}\, dt}\right) \tag{2}$$

Since the load current is the sum of the switching and linear regulator current,

$$I_{SR} = i_{load} - i_{LR} \tag{3}$$

Substitute equation (3) into equation (2),

$$I_{SR}^{*} = \text{argmax}_{I_{SR} \geq 0}\left(\frac{\int v_{load} \cdot i_{load}\, dt}{Vdd \int_{t:i_{LR}>0} i_{LR}\, dt + \int v_{load} \cdot (i_{load} - i_{LR})dt}\right) \tag{4}$$

Applying expansion,

$$I_{SR}^{*} = \text{argmax}_{I_{SR} \geq 0}\left(\frac{\int v_{load} \cdot i_{load}\, dt}{Vdd \int_{t:i_{LR}>0} i_{LR}\, dt + \int v_{load} \cdot (-i_{LR})dt + \int v_{load} \cdot (i_{load})dt}\right) \tag{5}$$

Since $\int v_{load} \cdot i_{load}\, dt$ term is known, maximizing η is the same as minimizing the following expression.

$$I_{SR}^{*} = \text{argmin}_{I_{SR} \geq 0}\{Vdd \int_{t:i_{LR}>0} i_{LR}\, dt + \int v_{load} \cdot (-i_{LR}) dt\} \quad (6)$$

Break up the integration into two segments: $\{t:i_{LR}>0\}$ and $\{t:i_{LR}<0\}$:

$$I_{SR}^{*} = \text{argmin}_{I_{SR} \geq 0}\{Vdd \int_{t:i_{LR}>0} i_{LR}\, dt + \int_{t:i_{LR}>0} v_{load} \cdot (-i_{LR}) dt + \int_{t:i_{LR}<0} v_{load} \cdot (-i_{LR}) dt\} \quad (7)$$

Collect terms corresponding to common time intervals:

$$I_{SR}^{*} = \text{argmin}_{I_{SR} \geq 0}\{\int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot i_{LR}\, dt + \int_{t:i_{LR}<0} v_{load} \cdot (-i_{LR}) dt\} \quad (8)$$

Equation (8) can be understood as the optimal switching regulator current maximizing η is equivalent to minimizing total energy loss. The first term in equation (8) is the energy loss when the linear regulator is sourcing current. The voltage drop is $Vdd - v_{load}$. The second term is the energy loss when the linear regulator is sinking current. Intuitively, whenever $Vdd - v_{load}$ is small, the linear regulator should be sourcing current. Whenever v_{load} is small, the linear regulator should be sinking current.

Restating the original objective, one gets:

$$I_{SR}^{*} = \text{argmin}_{I_{SR} \geq 0}(E_{loss}) = \text{argmin}_{I_{SR} \geq 0}\{\int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot i_{LR}\, dt + \int_{t:i_{LR}<0} v_{load} \cdot (-i_{LR}) dt\} \quad (9)$$

Express E_{loss} as a function of I_{SR}:

$$E_{loss} = \int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (i_{load} - I_{SR}) dt + \int_{t:i_{LR}<0} v_{load} \cdot (-i_{load} + I_{SR}) dt \quad (10)$$

More algebraic manipulation yield:

$$E_{loss} = \int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (-I_{SR})dt + \int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (i_{load})dt$$

$$+ \int_{t:i_{LR}<0} v_{load} \cdot I_{SR}\,dt + \int_{t:i_{LR}<0} v_{load} \cdot (-i_{load})dt \quad (11)$$

Collecting terms,

$$E_{loss} = \int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (-I_{SR})dt + \int_{t:i_{LR}>0} Vdd \cdot i_{load}\,dt +$$

$$+ \int_{t:i_{LR}<0} v_{load} \cdot I_{SR}\,dt + \int v_{load} \cdot (-i_{load})dt \quad (12)$$

Since $\int v_{load} \cdot i_{load}\,dt$ term is known and $\int_{t:i_{LR}>0} Vdd \cdot i_{load}\,dt$ is independent of I_{SR} to the first order,

$$I_{SR}^{*} = \text{argmin}_{I_{SR}\geq 0}(\int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (-I_{SR})dt + \int_{t:i_{LR}<0} v_{load} \cdot I_{SR}\,dt) \quad (13)$$

Denote the argmin parameter in Equation (13) as $\tilde{E}_{loss}$

$$\tilde{E}_{loss} = \int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (-I_{SR})dt + \int_{t:i_{LR}<0} v_{load} \cdot I_{SR}\,dt \quad (14)$$

Find the differential change in $\tilde{E}_{loss}$ when there is a differential change in I_{SR}

$$d\tilde{E}_{loss} = \int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (-dI_{SR})dt + \int_{t:i_{LR}<0} v_{load} \cdot dI_{SR}\,dt \quad (15)$$

Divide $d\tilde{E}_{loss}$ by dI_{SR},

$$\frac{d\tilde{E}_{loss}}{dI_{SR}} = \int_{t:i_{LR}>0} (Vdd - v_{load}) \cdot (-1)dt + \int_{t:i_{LR}<0} v_{load}\,dt \quad (16)$$

To find the minimum $\tilde{E}_{loss}$

$$\frac{d\tilde{E}_{loss}}{dI_{SR}} = 0 \tag{17}$$

This means that:

$$\int_{t:i_{LR}>0}(Vdd - v_{load}) \cdot (-1)dt + \int_{t:i_{LR}<0} v_{load}\, dt = 0 \tag{18}$$

Expand this equation:

$$\int_{t:i_{LR}>0} Vdd \cdot (-1)dt + \int_{t:i_{LR}>0}(v_{load})dt + \int_{t:i_{LR}<0} v_{load}\, dt = 0 \tag{19}$$

Collecting terms yields:

$$\int_{t:i_{LR}>0} Vdd \cdot (-1)dt + \int_{t=0}^{t=T} v_{load}\, dt = 0 \tag{20}$$

Rearranging yields,

$$\frac{\frac{1}{T}\int_{t=0}^{t=T} v_{load}\, dt}{Vdd} = \frac{\int_{t=0\ \&t:i_{LR}>0}^{t=T} 1dt}{T} \tag{21}$$

Instead of starting at time 0, we can start at time t_0,

$$\frac{\frac{1}{T}\int_{t=t_0}^{t=t_0+T} v_{load}\ dt}{Vdd} = \frac{\int_{t=t_0\ \&\ t:i_{LR}>0}^{t=t_0+T} 1dt}{T} \tag{22}$$

$$\frac{\textbf{average}\ (\mathbf{v_{load}})}{\mathbf{Vdd}} = \textbf{Duty Cycle}_{\textbf{Linear Regulator}} \tag{23}$$

The linear regulator duty cycle is defined as the fraction of time the linear regulator is sourcing current from the supply voltage. Hence (1 – Duty Cycle) is the fraction of time the linear regulator is sinking current to ground. Equation (23) says that when the average v_{load}

normalized by Vdd is equal to the linear regulator duty cycle, the total energy loss is at a minimum. The equality holds for any continuous and bounded i_{load} and v_{load} waveforms. Therefore, if the load impedance contains capacitance or inductance, the optimization equality (23) will still hold.

3.2 Simulation Results

Figure 3.3 is a block diagram of a linear regulator in parallel with a switching regulator. This simulation statically varies $I_{command}$ and measures the linear regulator duty cycle and total energy loss. The envelope signal, v_{load}, is a sample 802.11g envelope signal. This block diagram is simulated in Matlab Simulink. The inductor in the switching regulator is modeled as an ideal inductor with a value of 10uH. The switches in the switching regulator and the control block are modeled as an ideal square wave voltage source with a duty ratio that is dependent on the difference between i_{SR} and $I_{command}$. The inductor integrates the difference between v_{load} and the square pulse. The linear regulator current, i_{LR} is taken as the difference between i_{load} and i_{SR}. The linear regulator current, i_{LR} is then compared to zero and produces a square pulse that is 1 when $i_{LR} >= 0$ and 0 when $i_{LR} < 0$. The fraction of time that the square pulse is 1 is the linear regulator duty cycle. The linear regulator duty is the fraction of time that the linear regulator is sourcing current from the supply.

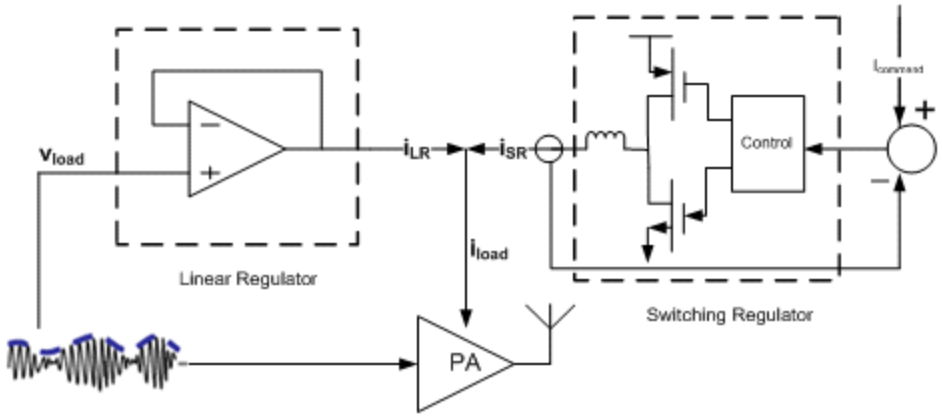

Figure 3.3 Parallel Hybrid Linear Switching Regulator

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Figure 3.4 plots the total energy loss versus the DC switching regulator current for a sample 802.11g envelope signal. One can see that at 1.55A of switching regulator current, the total energy loss is at a minimum. Figure 3.5 plots the linear regulator duty cycle versus the DC switching regulator current. On the same axes, the average v_{load} normalized by Vdd is also plotted. One can see that both curves intersect when the switching regulator current is 1.55A. This shows that at the minimum energy loss, the linear regulator duty cycle is equal to the average load voltage normalized by the supply voltage, Vdd.

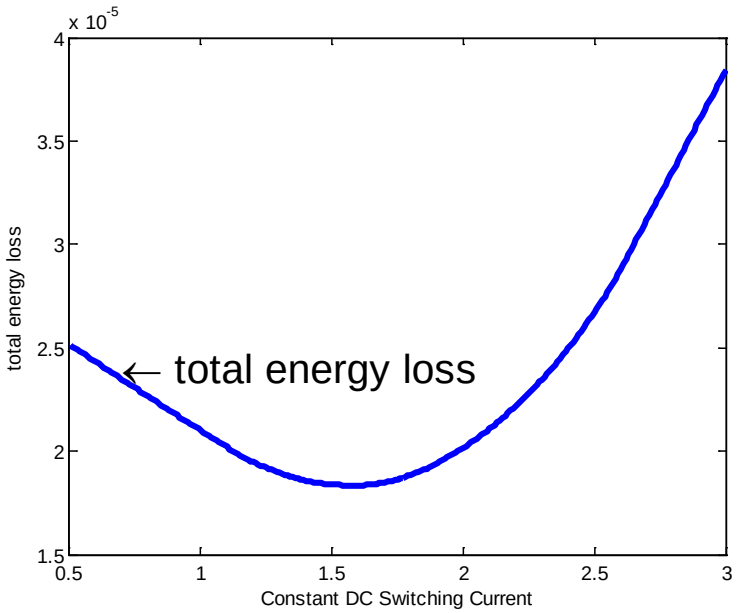

Figure 3.4 total energy loss versus I_{SR}

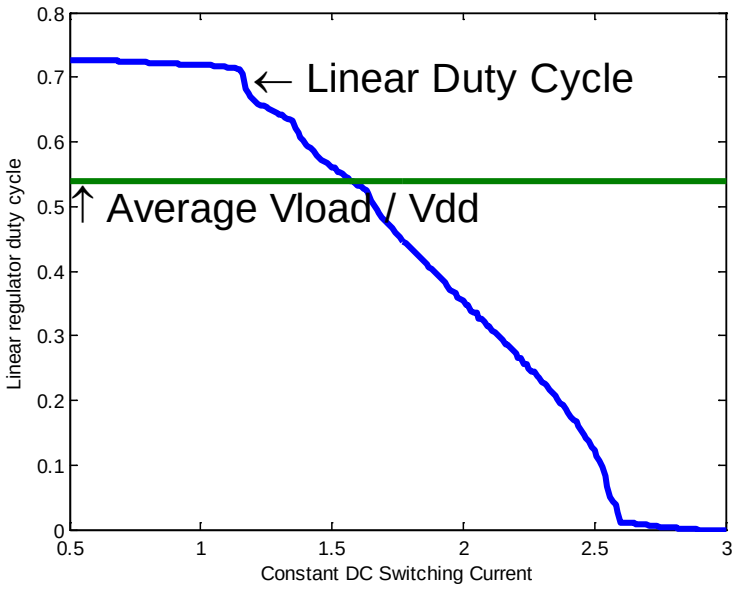

Figure 3.5 Linear Regulator Duty Cycle and Average v_{load} versus I_{SR}

3.3 Efficiency Optimization Architecture

Figure 3.6 shows a block diagram of an efficiency optimization scheme for the parallel hybrid linear switching regulator. Two measurements are made in this diagram: the average envelope load normalized by Vdd and the linear regulator duty cycle. The compensator takes the difference between the two measurements and outputs the desired current command, $I_{command}$ for the switching regulator. The compensator takes the form a proportional integrator controller. The bandwidth in the feedback loop determines the bandwidth of the switching regulator loop. If the switching regulator has a switching frequency of 2MHz, this bandwidth can be set around 200kHz.

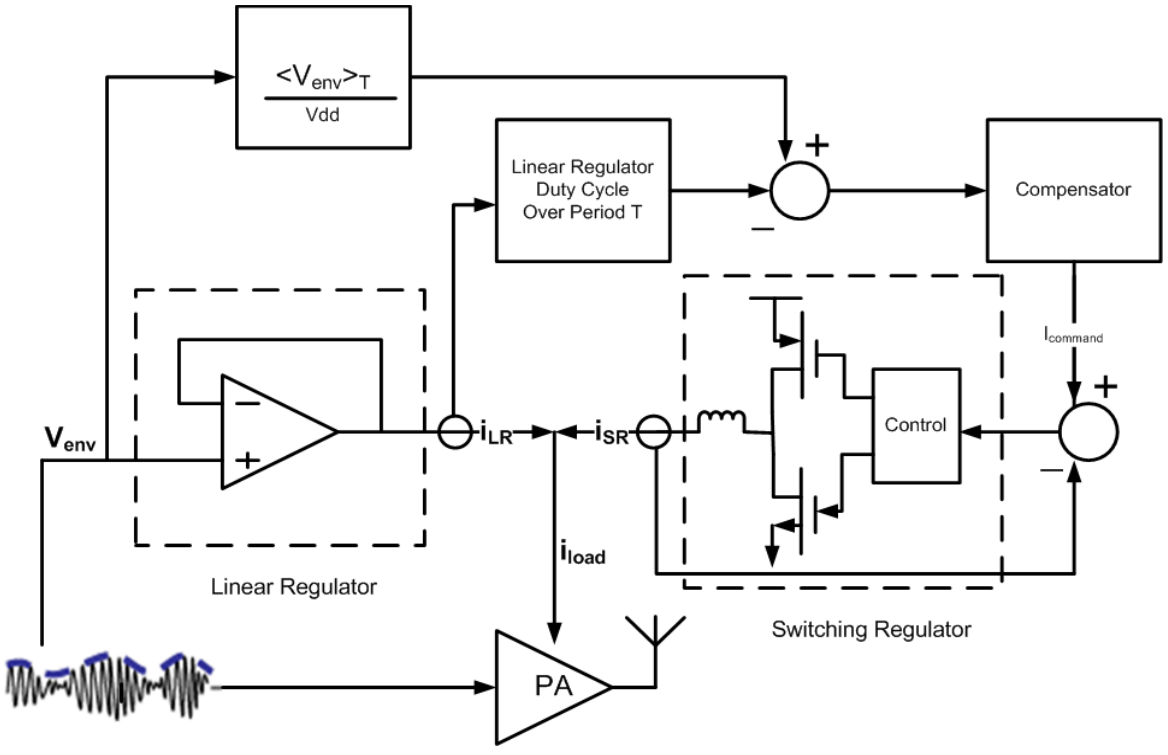

Figure 3.6 Parallel Hybrid Linear Switching Efficiency Optimization Architecture

3.4 Simulation Results

The hybrid regulator with optimization scheme in Figure 3.6 is simulated in Matlab Simulink. Similar to the simulation done in Figure 3.3, this simulation is done for a sample 802.11g envelope signal. The difference is that the optimization scheme automatically finds the correct $I_{command}$ to the switching regulator. The frequency spectrum of the envelope signal is shown in Figure 2.5. The inductor in the switching regulator is modeled as ideal. The switches and the control box are modeled as a square wave with a duty cycle proportional to the difference between $I_{command}$ and i_{SR}. The supply voltage is 3.6 volts. The switching frequency of the buck converter is 2MHz. The time window is 100us.

Figure 3.7 plots the linear regulator duty cycle and average Vout or Venv normalized by Vdd. The linear regulator duty cycle is the fraction of time that i_{LR} is greater than or equal to 0. One can see that over the course of time, these two values are very close together. Figure 3.8 plots the desired switching regulator current versus time. One can see that the desired switching regulator current centers around 0.3A. Figure 3.9 plots the cumulative efficiency of the regulator versus time. The efficiency settles around 80%. This efficiency simulation assumes that the switching regulator is 100% efficient and the linear regulator introduces loss from sourcing and sinking current. Despite wide voltage swing of the envelope signal, efficiency still remains high, at 80%. This shows that if the optimization scheme is employed, the overall efficiency depends mostly on the efficiency of the low-bandwidth switching regulator. Figure 3.10 plots the sample 802.11g envelope signal.

The next set of graphs is plotted under the case when the finite averaging time window is replaced by a low pass filter. Here the envelope voltage and the instantaneous linear regulator

duty cycle are low passed by a 2^{nd} order filter at ω_o = 20KHz. Figure 3.11 plots the low passed linear regulator duty cycle and the low passed Vout/Vdd. One can see that the linear regulator duty cycle does track Vout/Vdd. Figure 3.12 plots the desired switching regulator current. Again the desired switching current centers at 0.3A. Figure 3.13 plots the cumulative efficiency, which settles around 80%. Figure 3.14 plots the same envelope signal as Figure 3.10.

The efficiency optimization architecture is also simulated for $<Vout>_{ave}$/Vdd that is around 0.6. The same 802.11g envelope signal is rescaled and plotted in Figure 3.18. Again, Figure 3.15 shows that the linear regulator duty cycle does track averaged normalized Vout. Figure 3.16 plots the desired switching regulator current. The current is around 1A. Figure 3.17 plots the cumulative efficiency, which settles around 93%.

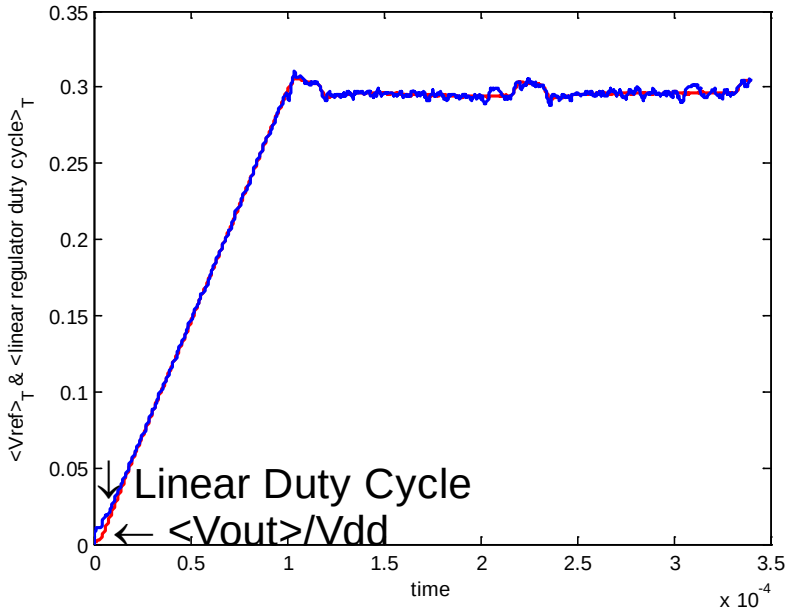

Figure 3.7 Linear Regulator Duty Cycle and Average Vout/Vdd versus time (Rectangular Time Window)

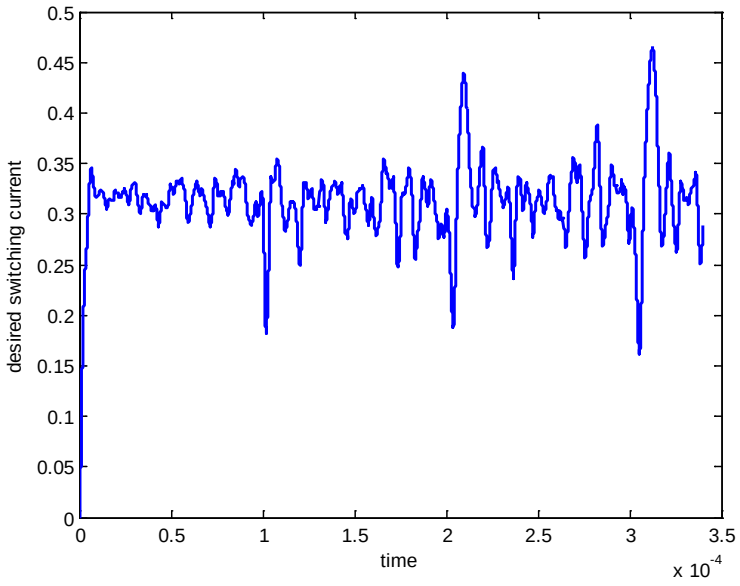

Figure 3.8 Switching Regulator Current Command versus time

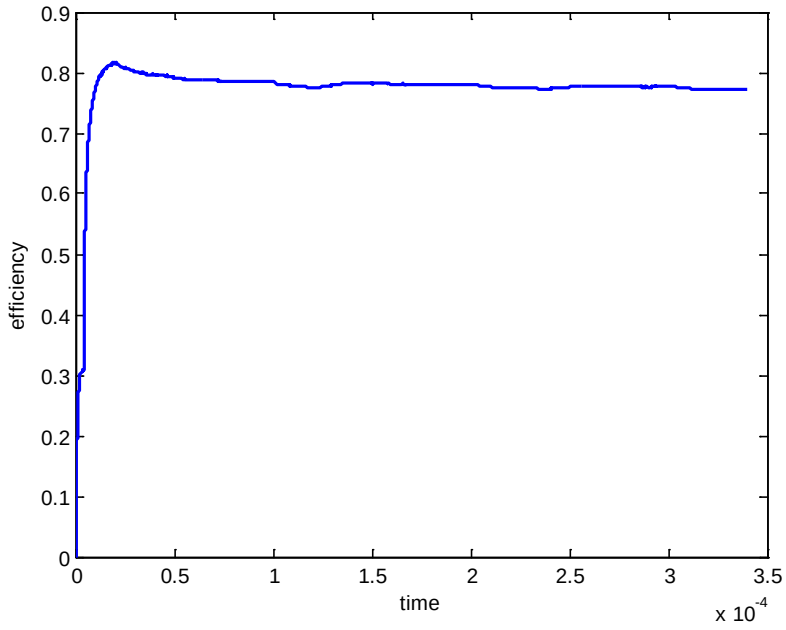

Figure 3.9 Cumulative Efficiency versus Time

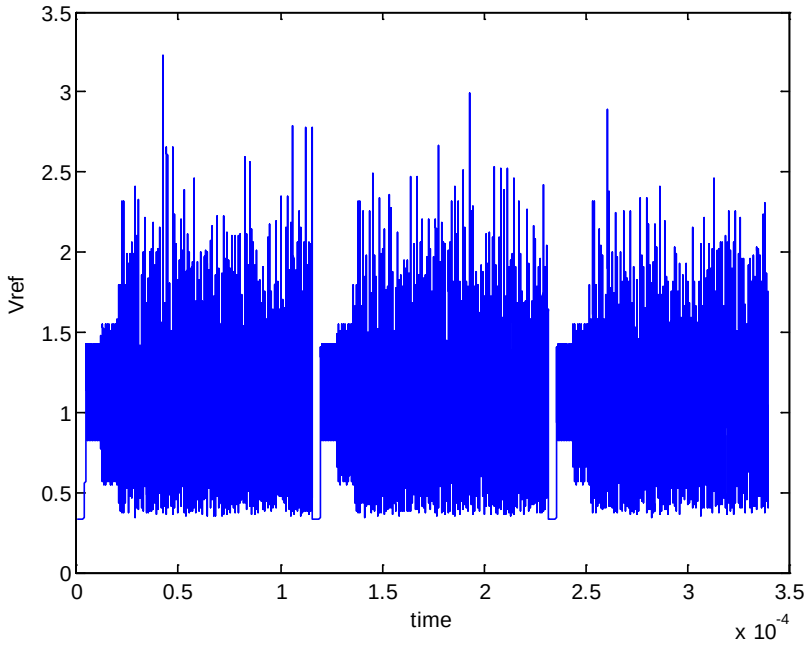

Figure 3.10 802.11g Envelope signal

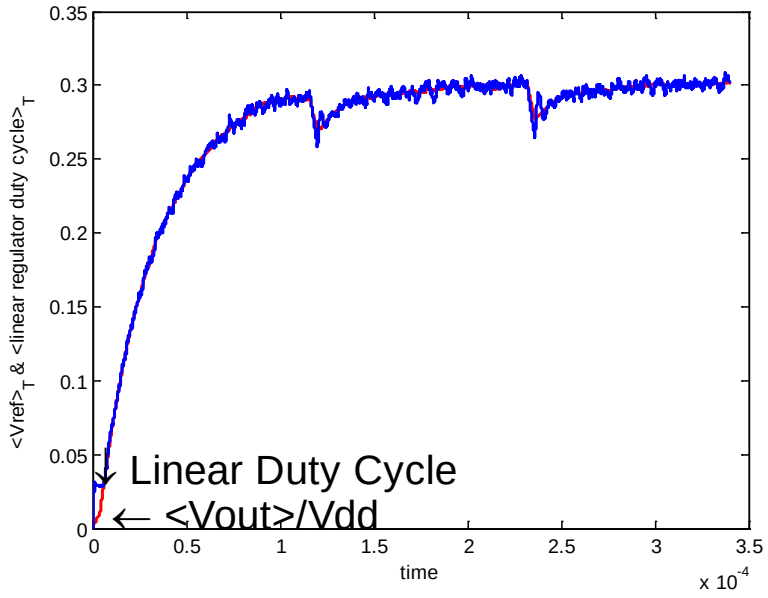

Figure 3.11 Linear Regulator Duty Cycle and Average Vout/Vdd versus time

(Low Pass Filtering of Duty Cycle)

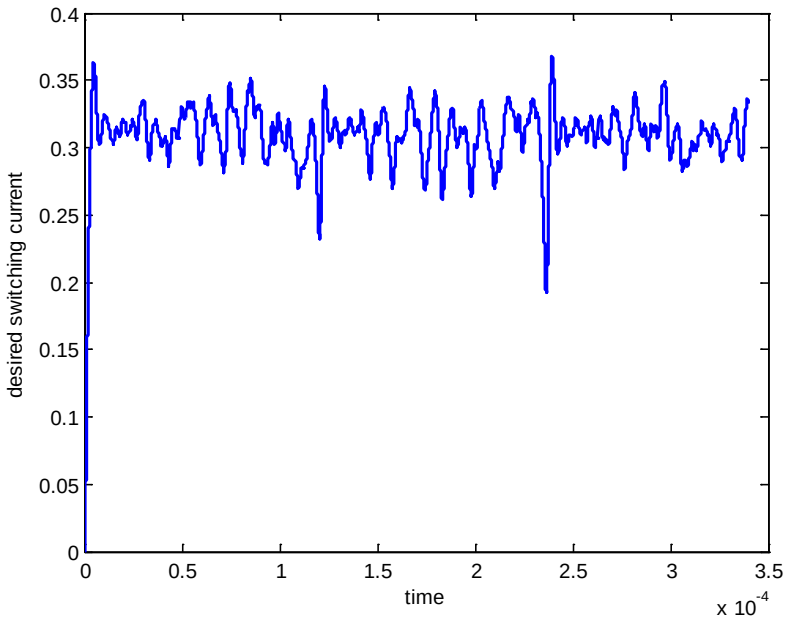

Figure 3.12 Desired Switching Regulator Current Command versus time

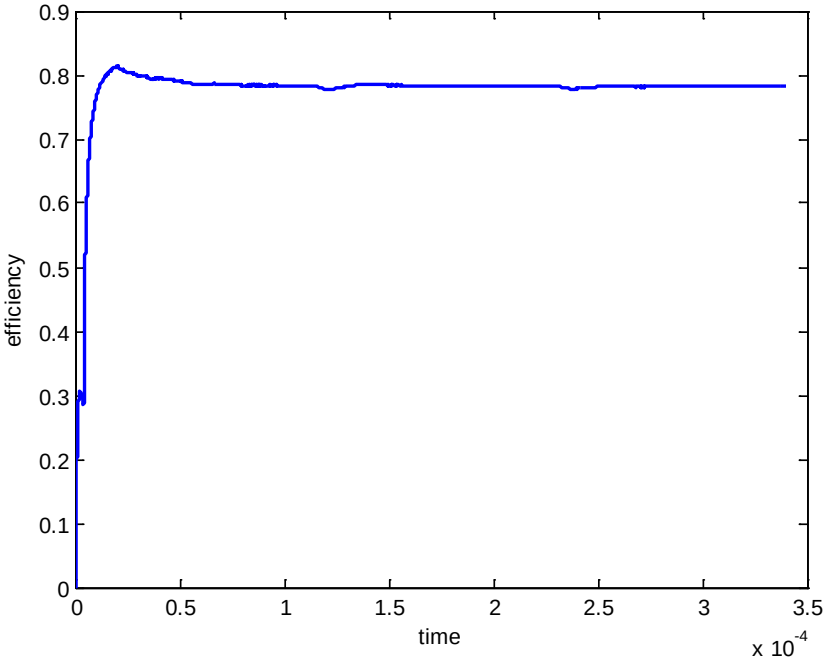

Figure 3.13 Cumulative Efficiency versus Time

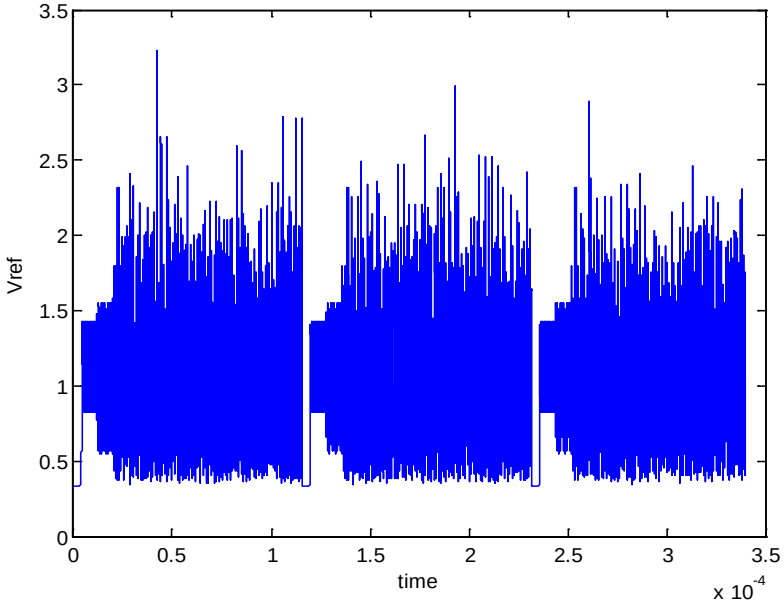

Figure 3.14 802.11g Envelope signal

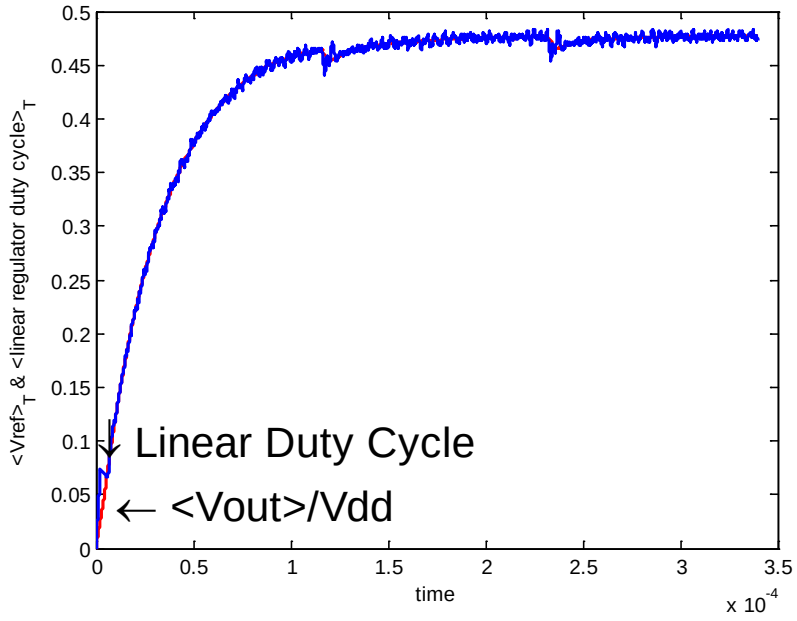

Figure 3.15 Linear Regulator Duty Cycle and Average Vout/Vdd versus time

(Low Pass Filtering of Duty Cycle)

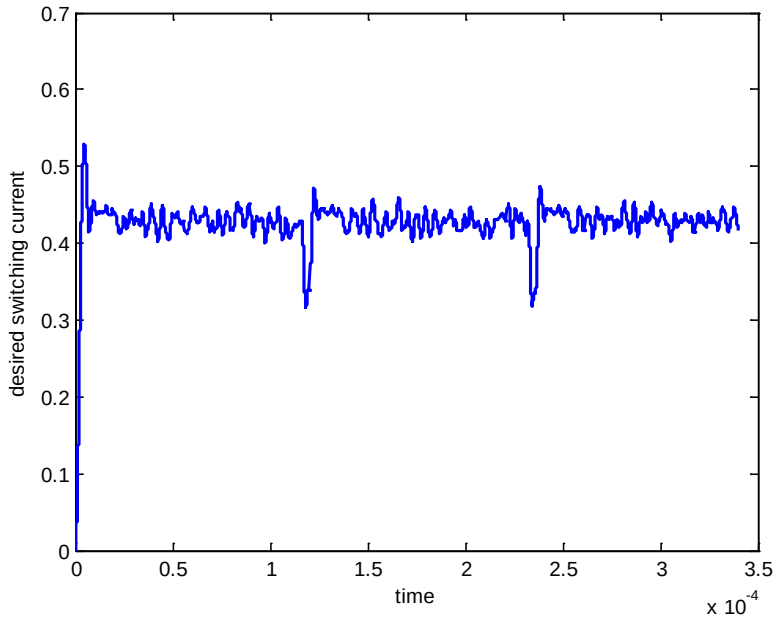

Figure 3.16 Desired Switching Regulator Current Command versus time

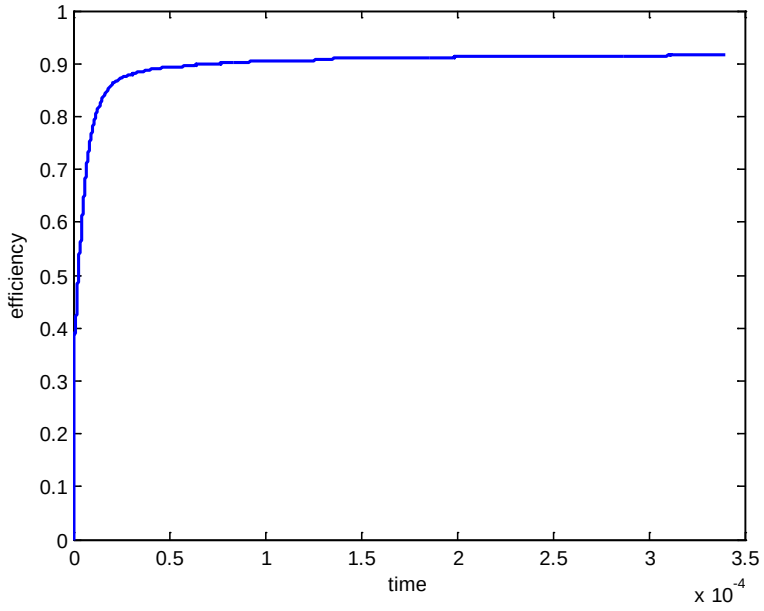

Figure 3.17 Cumulative Efficiency versus Time

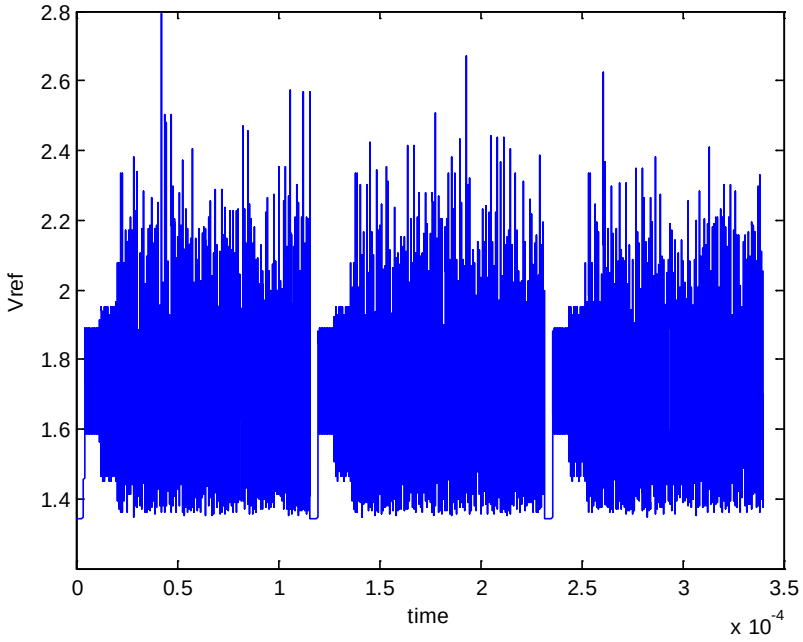

Figure 3.18 802.11g Envelope signal

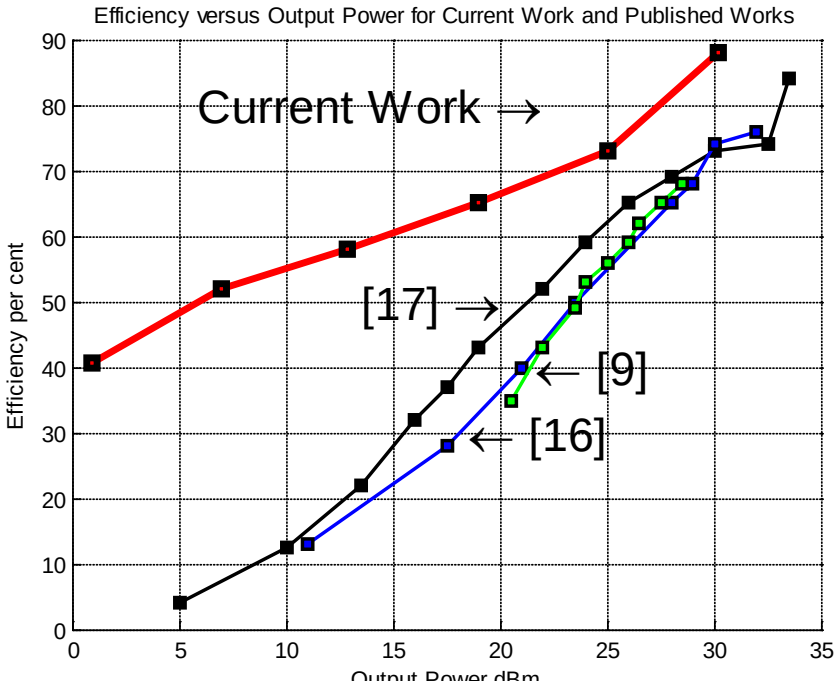

Figure 3.19 Efficiency of Current Regulator versus Other Works versus Output Power

Figure 3.19 compares the efficiency of the proposed hybrid regulator and other published results versus output power. The switching regulator in the proposed work is assumed to be 95% efficient for all output power. The curve for reference [17] shows the efficiency of a conventional hybrid linear switching regulator with a 10MHz bandwidth. The curve for reference [16] shows the efficiency of a wideband switching regulator with a 5MHz bandwidth. The curve for reference [9] shows the efficiency of a series hybrid linear switching regulator with a 4MHz bandwidth. The output power of the proposed regulator is varied by changing the amplitude and dc bias of the same 802.11g envelope signal. Efficiency of the hybrid regulator is simulated using MATLAB Simulink as done previously. One can notice significant efficiency improvement at lower output power.

Chapter 4

Envelope Amplifier Design

The goal of the experimental component of this project is to design, fabricate, and test the entire hybrid regulator with optimization control. The first part designed is the linear regulator. The targeted wireless standard is 802.11g. Figure 2.5 shows the envelope spectrum and the in-phase (I) spectrum of a sample 802.11g waveform. The bandwidth of the envelope amplifier is chosen to be 20MHz because the frequency component of the envelope signal at 20MHz is around 50dB lower than the peak at DC. A bandwidth of 20MHz should be more than sufficient to capture almost all of the energy in the signal.

The supply impedance of a Class B single ended PA can be approximated as a linear resistor. This is because a Class B PA is nominally biased such that its main transistor conducts zero current. As the input voltage swing increases, the average current in the PA increases proportionally. In the envelope tracking or polar architecture, the supply voltage varies in synchronization with the gate envelope voltage. Hence the supply impedance is also approximated as a linear resistor. Suppose the designed Class B PA has a maximum output power of 1W and a supply voltage of 3.6V. Since the efficiency of an ideal Class B PA is 78%, the current required into the supply is 350mA. Hence the linear regulator is designed to sink and source 500mA, enough to meet the required current. Depending upon the transistor sizing and supply voltage to gate voltage ratio, the supply impedance vary in the range of a few ohms. A value of 4 Ω is chosen based on a nominally designed class B PA.

The targeted unity gain bandwidth is 300MHz in order to track a 20MHz bandwidth signal. This will provide a loop gain greater than 10 at 20MHz giving an error less than 10% at 20MHz. At the crossover point when the linear regulator is not providing current to the load, the linear regulator should source and sink 10mA of current. A current of 10mA at crossover gives a 98% current efficiency while providing enough transconductance to allow for adequate tracking and crossover current control. The detailed analysis is calculated later in the chapter. The rest of the targeted specifications are summarized in the table below.

4.1 Specifications

Specifications	Targeted Value
Supply Voltage	3.6V
Output Voltage	Rail-to-Rail
Output Current	Sinks 500mA and sources 500mA
PA load	4Ω
Unity Gain Bandwidth	300MHz
Crossover Current	10mA
Technology	0.18um CMOS

4.2 List of Constraints

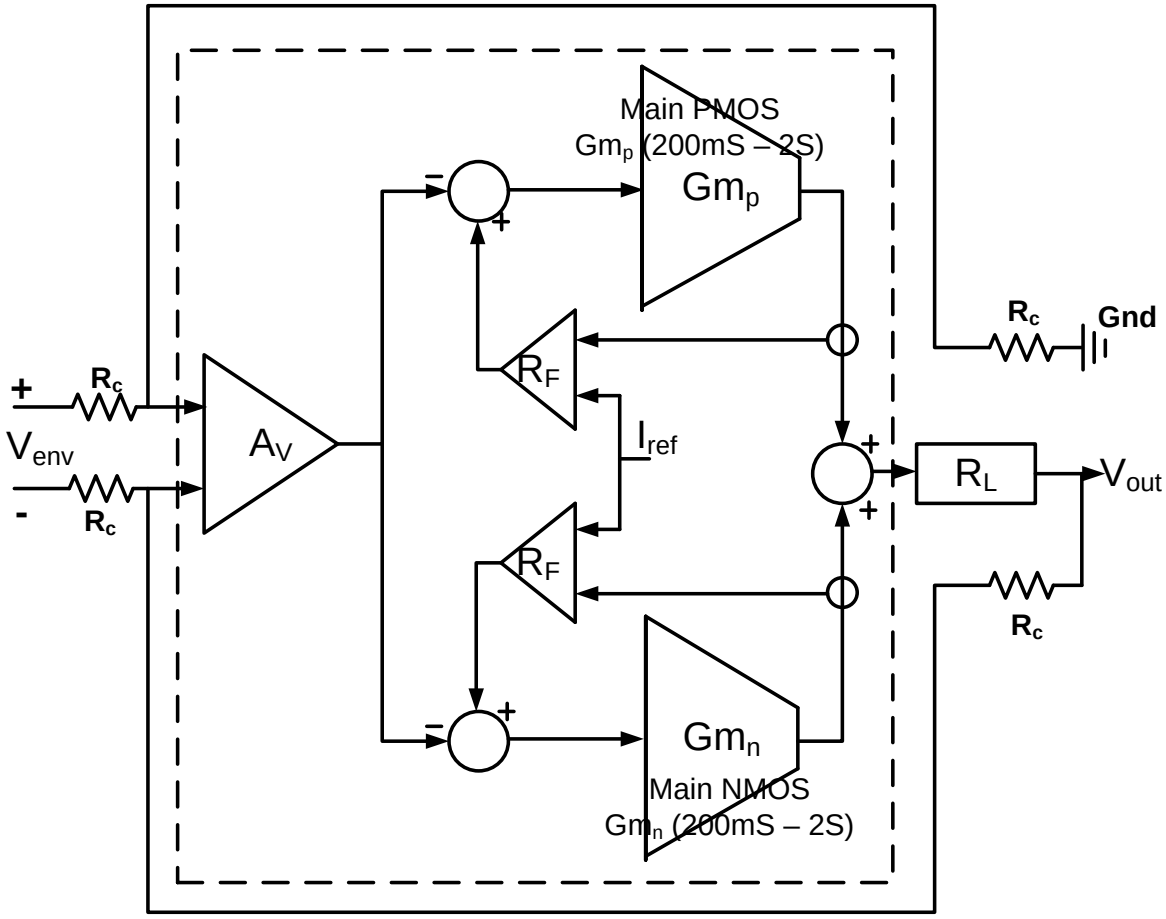

Figure 4.1 Block Diagram of the Linear Regulator

Figure 4.1 is a simplified block diagram of the designed linear regulator. The dashed line contains what is on chip and resistors R_c are appropriate feedback resistors. The transconductance of the main PMOS and NMOS transistors are denoted as Gm_p and Gm_n. The PA supply load impedance is denoted as R_L, 4 Ω. The desired cross-over current that the main PMOS and NMOS transistors conduct is denoted as I_{ref}. The minor loop consisting of $Gm_p(Gm_n)$ and R_F is used for controlling crossover current. With applied voltage of zero, Gm_p and Gm_n are commanded in closed minor loop to each provide 10mA. The major loop consisting of A_V, Gm_p (Gm_n) and R_L is used for tracking.

At maximum current, current of the main PMOS or the main NMOS transistor, Ip or In respectively is equal to 500mA. The targeted overdrive voltage of the main transistors, Vov is equal to 500mV. Through Cadence simulation under different corners, a good PMOS (NMOS) transistor size with Vov of 500mV and 500mA of current is 10mm (5mm). Cadence simulations show that at the typical corner and maximum current of 500mA, the transconductance of the main transistors is 2S. At crossover, current through the main PMOS transistor (Ip) is equal to 10mA. Simulations show that the gate to source voltage, Vgs is around 200mV with a threshold voltage of around 500mV. This means that when the currents though the main transistors becomes 10mA, the transistors are operating in the sub-threshold domain. Cadence simulations show that the minimum Gm_p and Gm_n at the typical corner is 200mS.

A set of constraints that need to be met for crossover current control, tracking and stability is as follows.

Constraint #1

At crossover, the crossover current is 10mA. A current error of ±1mA can be tolerated leading to a loop gain of at least 10.

$$R_F \cdot Gm_{pmin} > 10 \rightarrow R_F > 50\Omega$$

Constraint #2

Input voltage V_{env} is around a few volts. A voltage error of tens of mVolts can be tolerated leading to a loop gain of at least 100. At crossover of the class AB stage, in order to have voltage tracking accuracy of 1%, loop gain must be greater than 100

$$A_V \cdot R_L \cdot \frac{\mathrm{Gm_{pmin}}}{1 + \mathrm{Gm_{pmin}} \cdot \mathrm{R_F}} > 100$$

$$\rightarrow A_V \cdot R_L \cdot \frac{1}{\mathrm{R_F}} \gtrsim 100 \;\; since \;\; R_F \cdot Gm_{pmin} > 10$$

$$\rightarrow A_V > 1300$$

Voltage gain A_V is the gain from the voltage input command V_{env} to the gate of the main PMOS (NMOS) transistor. For 0.18um technology, $g_m r_o$ is around 10. Four stages of $g_m r_o$ are needed to provide adequate loop gain.

$$(g_m r_o)^4 \gg A_V = 1300$$

When either of the main transistors (NMOS or PMOS) is fully on, the minor loop is cut off. This fact will be explained later. Loop gain becomes

$$A_V \cdot Gm_p \cdot R_L > A_V \cdot Gm_{pmin} \cdot R_L = 1300 \cdot 0.2 \cdot 4 = 1040 \gg 100$$

A loop gain of 1040 is more than enough for 1% for voltage tracking accuracy when not at crossover.

Constraint #3

At maximum current load, Ip (In) = 500mA. GBW = 300MHz as specified in the specification table.

4.3 Transistor Level Circuit

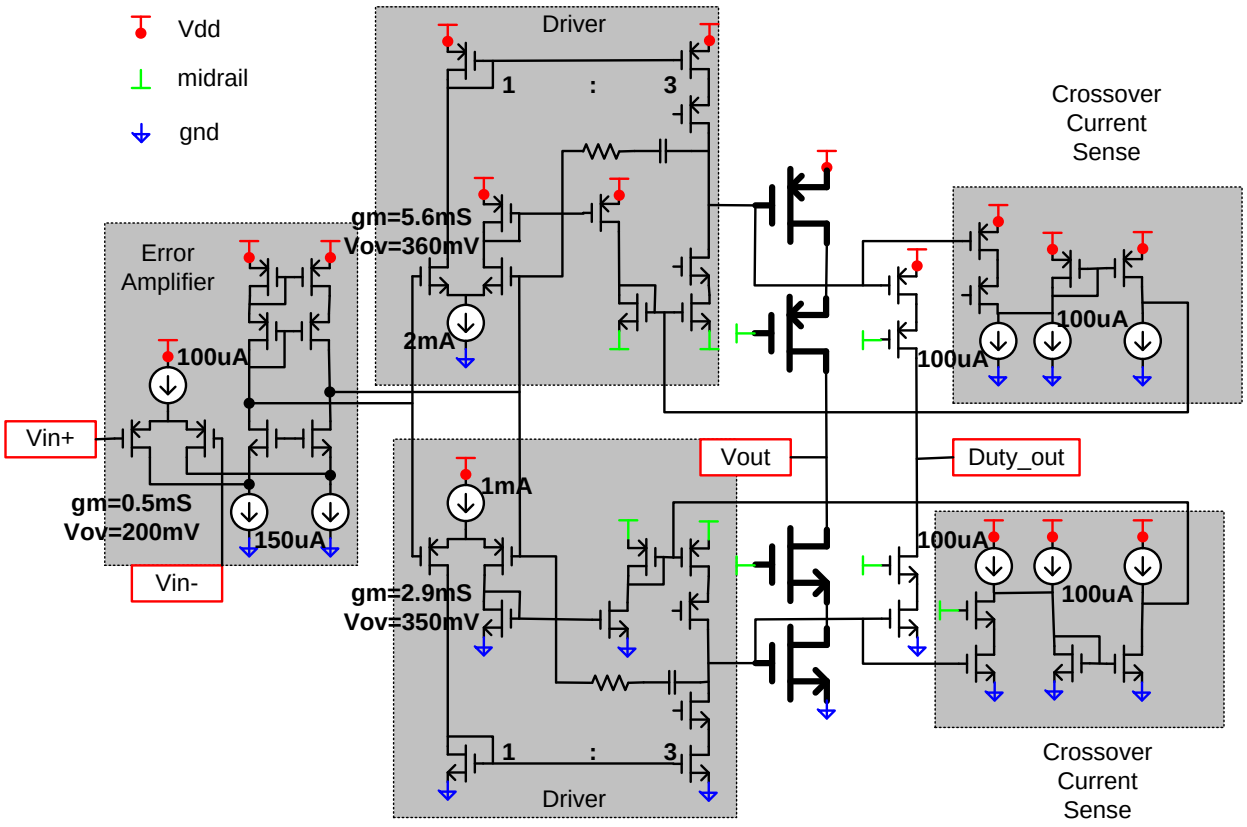

Figure 4.2 Simplified Transistor Level Circuit

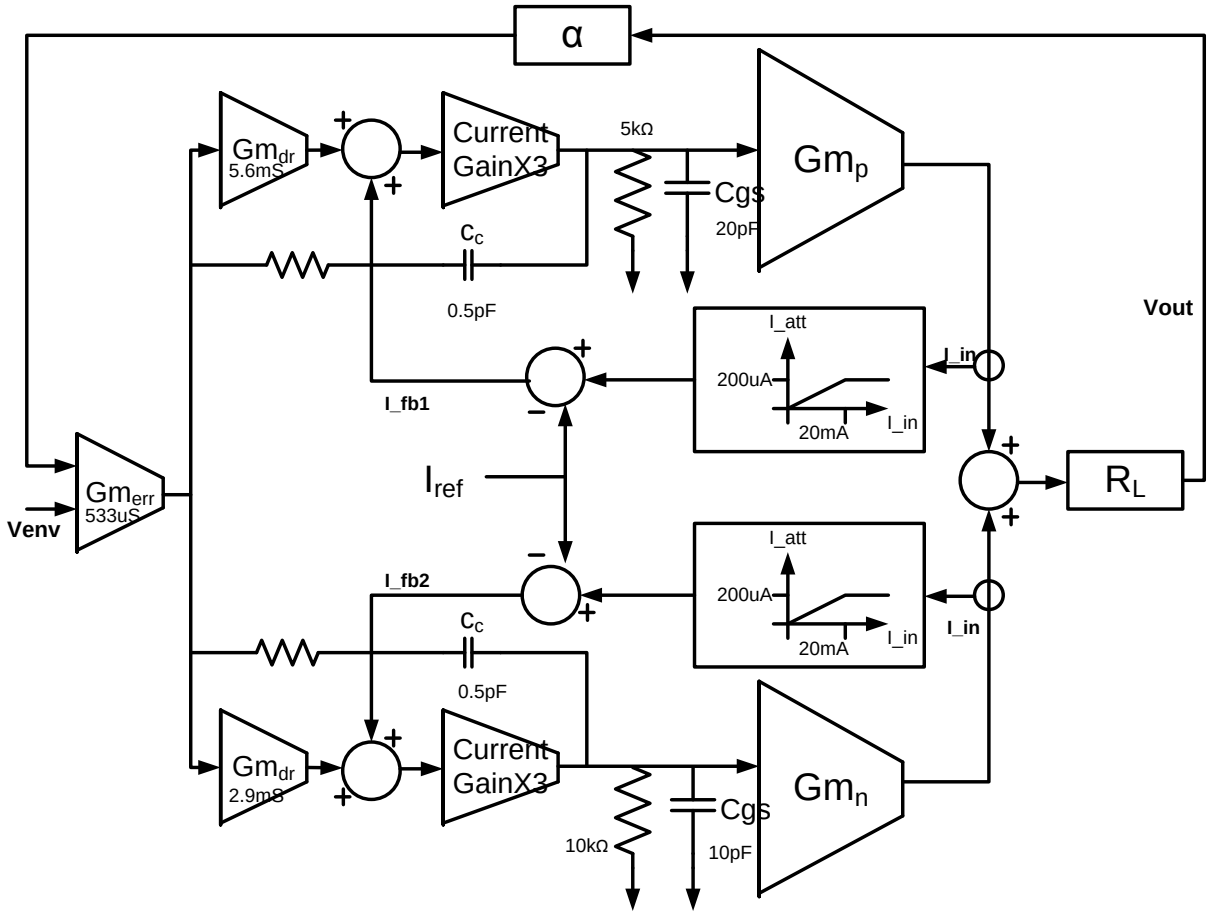

Figure 4.3 Detailed Block Diagram of Linear Regulator

Figure 4.2 shows a simplified transistor level schematic of the designed linear regulator. Figure 4.3 shows a more detailed block diagram of the linear regulator. This section will first discuss the design methodology of the linear regulator. Later this section will discuss the transistor level implementation.

The linear regulator contains five main parts: error amplifier, drivers for the main transistors, main PMOS and NMOS transistors, crossover current senses, and mirrors of the main transistors for duty cycle monitoring. The supply voltage of the regulator is 3.6V (indicated by the red symbol in Figure 4.2) and the midrail is 1.8V (indicated by the green symbol). Since the linear regulator is designed in 0.18um CMOS technology, the maximum tolerable Vgs and Vgd is 2V. This means that transistors need to be connected in series to reduce voltage stress. The main PMOS and NMOS transistors are cascoded with a transistor of equal size so that both transistors can be designed to share a junction. The gate voltage of the cascodes is biased at midrail. The driver for the main PMOS transistor is designed between the Vdd rail and the midrail. On the other hand, the driver for the main NMOS transistor is designed between the midrail and ground. The purpose of the midrail for driver is to limit voltage stress and also to reuse the bias current of the upper driver.

Given the size of the main PMOS (NMOS) transistor, the gate-to-source capacitance C_{gs} is simulated in Cadence to be 20pF (10pF). The driver block in the transistor diagram is equivalent to the cascoded Gm_{dr} and Current Gain blocks in the block diagram Figure 4.3. The driver schematic for the main PMOS transistor is shown in Figure 4.4. Each of these blocks is designed to operate as a purely linear function with high bandwidth.

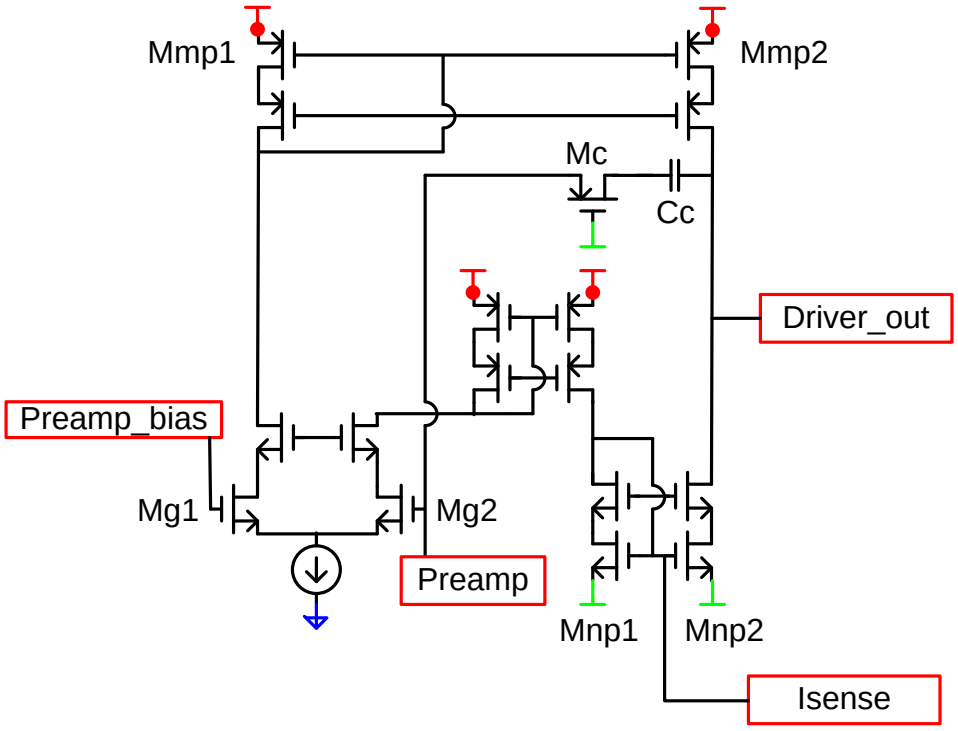

Figure 4.4 Driver for main PMOS

The schematic node Driver_out connects to the gate of the main PMOS transistor. The details of the driver will be discussed later. The driver needs to provide adequate current to drive the 20pF C_{gs} at a sine wave of 20MHz (envelope signal bandwidth) with 1 volt amplitude (typical maximum gate voltage swing). The peak current the driver needs to provide is 2.5mA. As mentioned in Constraint #2, four stages of $g_m r_o$ are required to provide adequate loop gain for voltage tracking accuracy. The output of the driver stage can only provide two stages of $g_m r_o$ due to voltage headroom restriction. This is because the output voltage of the driver is nominally biased close to the supply rail such that the main PMOS transistor is sometimes operating under the sub-threshold domain. With a bias current of 3mA, two stages of $g_m r_o$, and a channel length of 0.18um, the output impedance of the driver is 5kΩ. A two-stage miller compensated amplifier can provide compensation. The two-stage amplifier is formed by the error amplifier and the driver as shown in Figure 4.2. Correspondingly, the two stage amplifier is shown in the block

diagram Figure 4.3 as Gm_{err} (533uS), Gm_{dr} (5.6mS), and Current Gain (3X). Capacitance Cc (0.5pF) is the miller compensation capacitor. These numbers will be explained later. For now, let's calculate the GBW product of the amplifier. The symbol α is the feedback attenuation factor (½ explained later) which is shown both in Figure 4.1 and Figure 4.3.

$$GBW = \frac{Gm_{err}}{2C_c} \cdot Gm_{pmax} \cdot R_L \cdot \alpha \cdot \frac{1}{2\pi} = \frac{0.533m}{2 \cdot 0.5p} \cdot 2 \cdot 4 \cdot \frac{1}{2} \cdot \frac{1}{2\pi} = 340MHz$$

$$2nd\ pole\ freq = \frac{Gm_{driver} \cdot Current\ Gain}{C_{gs}} \cdot \frac{1}{2\pi}$$

$$= \frac{5.6m \cdot 3}{20p} \cdot \frac{1}{2\pi} = 130MHz$$

The 2nd pole is located at 130MHz and a compensation resistor R_z is used to introduce a left half plane zero to improve the phase degradation caused by the 2nd pole. The zero occurs at frequency:

$$\omega_z = \frac{1}{C_c \cdot [(Gm_{driver} \cdot Current\ Gain)^{-1} - R_z]} = -2\pi \cdot 130MHz$$

$$R_z = 2.5k\Omega$$

The resistor R_z is implemented by transistor Mc in triode in Figure 4.4. The 3rd order poles are the 1X3 mirror poles associated with the driver in Figure 4.4. The pole frequency is $\frac{f_T}{4}$ typically located around 500MHz giving an overall phase margin of 30 to 50 degrees.

The block diagram in Figure 4.3 also shows the minor loop that controls the crossover current. The minor loop consists of the current attenuation block, Current Gain Block and the transconductance of the main PMOS (NMOS) transistor. The current attenuation block measures

the main PMOS transistor current and produces a current that is 1/100th of the main PMOS current. This ratio is chosen so that the current sense does not use excessive amount of current.

$$T_{minor\ \ loop} = Current\ Attenuation \cdot Current\ Gain \cdot Rout_{driver} \cdot Gm_{pmin}$$

$$= 0.01 \cdot 3 \cdot 5k\Omega \cdot 200m = 30$$

The current attenuation block has a saturation point at 20mA of sense current and has a maximum output current of 200uA. This saturation point is necessary because as the main PMOS transistor conducts more current, the current attenuation block will produce too much current saturating the current gain block. The saturation point of 20mA is chosen because the nominal crossover current is 10mA. A 20mA saturation point gives enough current.

Constraint #2 needs to be checked. At crossover, major loop gain should be greater than 100. $Rout_{err}$ is the output impedance of the error amplifier:

$$\mathrm{T_{major\ loop}} = \mathrm{Gm_{err}} \cdot \mathrm{Rout_{err}} \cdot \frac{\mathrm{Gm_{dr}}}{\mathrm{Current\ Sense\ Gain}} \cdot \mathrm{R_L} \cdot \alpha$$

$$\mathrm{T_{major\ loop}} = 0.533\mathrm{mS} \cdot 1\mathrm{M\Omega} \cdot \frac{5.6\mathrm{mS}}{0.01} \cdot 4 \cdot \frac{1}{2} = 560 > 100$$

Error Amplifier

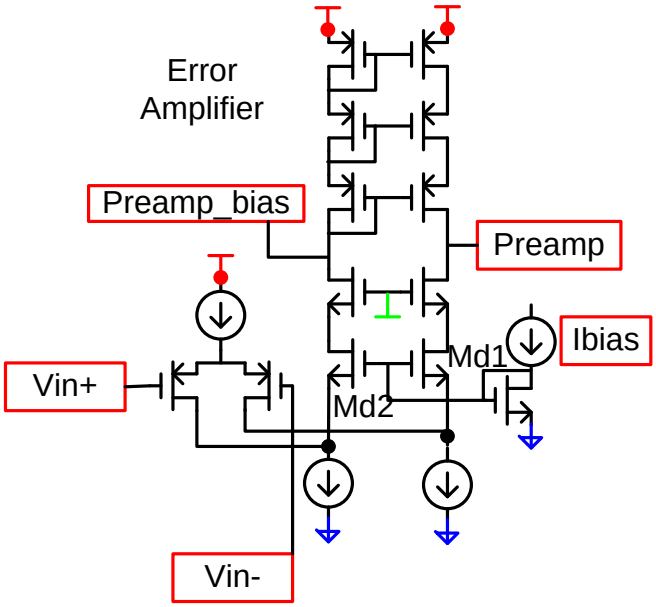

Figure 4.5 Error Amplifier Circuit Diagram

Figure 4.5 shows a transistor schematic of the error amplifier. Nodes Vin+ and Vin- are the positive and negative input terminals of the linear regulator. Output nodes Preamp and Preamp_bias are the inputs to the drivers for the main transistors. A folded-cascode structure is used here to improve the common-mode input range. The output of the linear regulator swings from gnd to Vdd and the feedback factor is ½. This means that the input common-mode range is from gnd to midrail. Furthermore, the error amplifier output structure is cascoded twice to increase the output impedance, r_o of the amplifier, thereby increasing the DC gain. The gates of transistors Md1 and Md2 are biased by a diode connected transistor. The current sources are mirror copies of a current reference. The transconductance of the error amplifier is 533uS and the output impedance is 1MΩ providing a gain of 533.

Driver

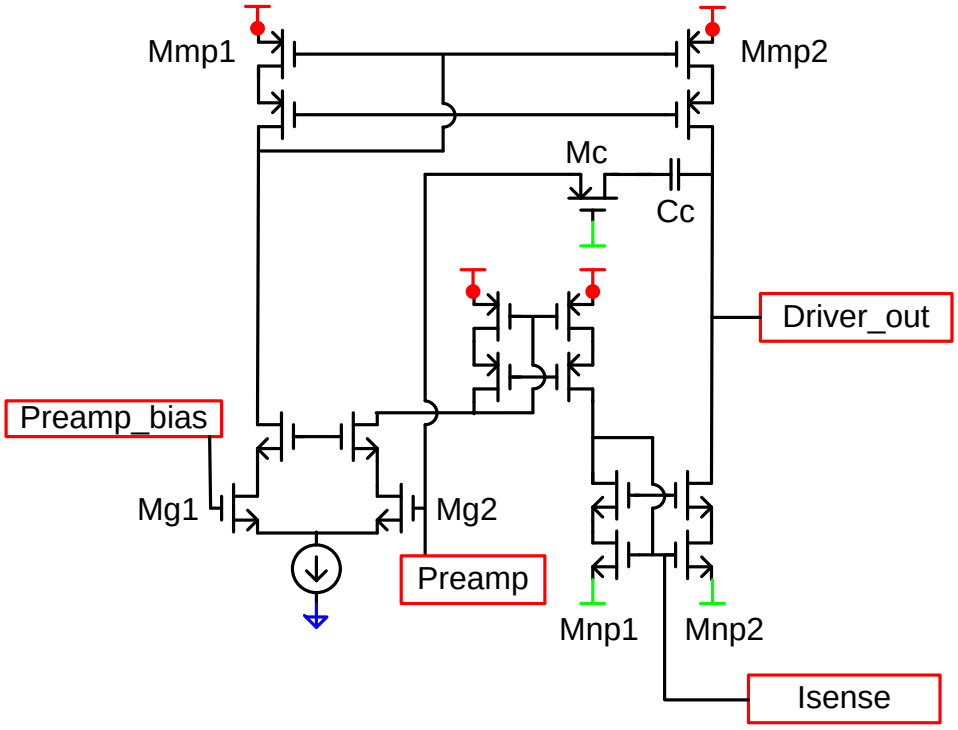

Figure 4.6 Driver for main PMOS

Figure 4.6 shows a transistor level schematic of the driver circuit for the main PMOS. Node Driver_out drives the gate of the main PMOS transistor. Nodes Preamp_bias and Preamp are the output nodes of the error amplifier. Node Isense is the output of the current sense block that forms the minor loop that controls the crossover current. The driver for the main NMOS transistor is very similar to this architecture. Transistors Mg1 and Mg2 form the transconductance gm stage which is a differential pair. The tail current is a mirror copy of a current reference. Transistors Mmp1 and Mmp2 (Mnp1 and Mnp2) form a 1:3 mirror. This mirror is used to allow reduced the bias current in the transconductance gm stage. A 1:3 mirror is chosen to decrease bias current in the gm stage while achieving sufficiently high frequency mirror poles. The tail current is set to 2mA which sets a bias current of 3mA in the transistors

Mmp2 and Mnp2. A wide-swing cascode is implemented here in order to increase the swing at the output of the driver. In order to run the main PMOS transistor at 10mA, the gate voltage needs to swing 200mV below the threshold voltage. The gate voltages of the wide swing cascodes are biased with a diode connected transistor with current coming from a current reference cell. Capacitor Cc is a compensation capacitor in the two-stage miller compensated amplifier which consists of the error amplifier and the driver. Transistor Mc is a transistor in triode to implement the compensation resistor to get adequate phase margin. The transconductance of the driver is 5.6mS for the upper driver and 2.9mS for the lower driver. The output impedance of the upper driver is 5kΩ and the output impedance of the lower driver is 10kΩ. This provides a gain of 80 for both of the drivers.

Crossover Current Sense

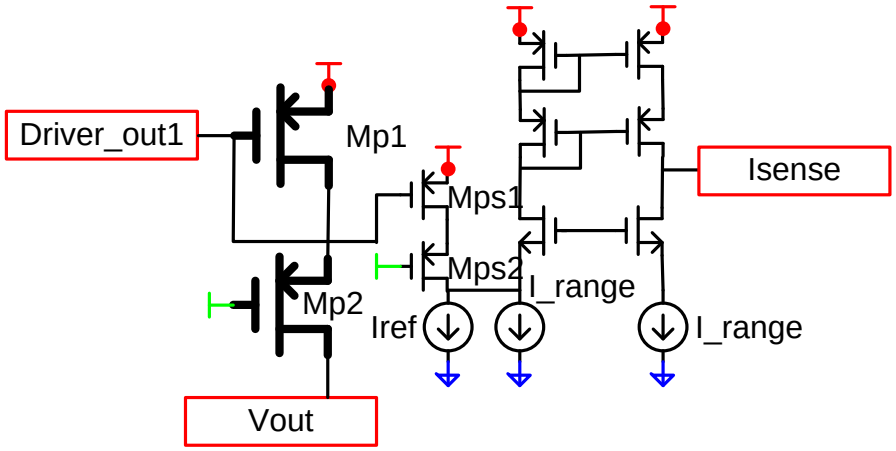

Figure 4.7 Crossover Current Sense

Figure 4.7 shows a transistor schematic of the crossover current sense. Current source Iref is the desired crossover current. Current source I_range helps define the saturation point, beyond which the current sense block saturates. Current sources Iref and I_range are set to 100uA. This gives a saturation point of 20mA in the main PMOS transistor since transistors Mp1 and Mps1 form a 100:1 current mirror. The width of transistor Mps1 is 1/100th of the width of transistor Mp1. In order to have functional current sense, the matching of Mp1 and Mps1 is very important. In addition, transistors Mp2 and Mps2 are cascodes which are used to reduce voltage stress and to help drain-to-source voltage Vds matching of Mp1 and Mps1. When current in Mp1 is very large, output node Isense sinks a saturated current of I_range. When the current in Mp1 is zero, output node Isense sources a saturated current of Iref.

Main Transistors and Linear Regulator Duty Cycle

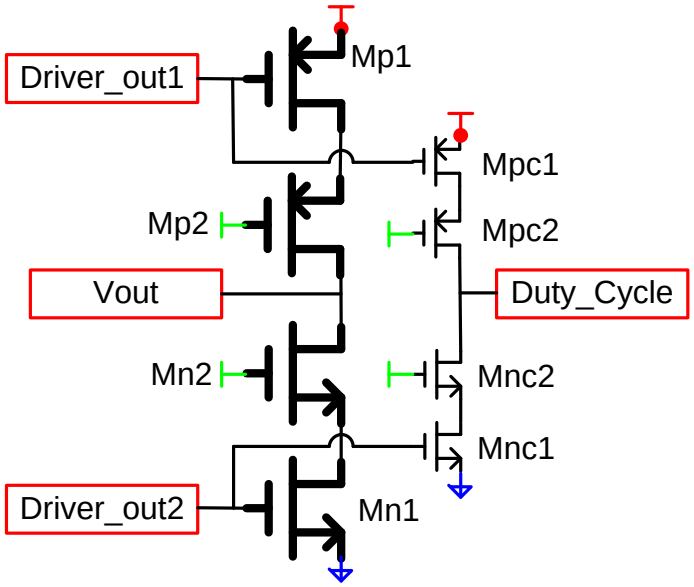

Figure 4.8 Linear Regulator Duty Cycle Circuit Diagram

Figure 4.8 shows a transistor schematic of the main transistors and linear regulator duty cycle extraction circuit. Transistors Mp1, Mn1, Mp2, and Mn2 are the main transistors and their cascode transistors. Transistors Mpc1, Mpc2, Mnc2, Mnc1 are mirror copies of transistors Mp1, Mp2, Mn2, and Mnc1. The width of transistor Mpc1 is $1/100^{th}$ of the width of transistor Mp1. The Duty_Cycle node is connected to a high impedance node. If the current in transistor Mpc1 is greater than the current in transistor Mnc1, the Duty_Cycle node will be pulled high. If the current in Mpc1 is less than the current in Mnc1, the Duty_Cycle node will be pulled low. Obviously, this depends on the matching of Mpc1 and Mp1 and Vds matching of the two transistors. Transistors Mp2 and Mpc2 are cascode transistors which help Vds matching of Mp1 and Mpc1. Simulations have shown that a simple cascode is adequate for Vds matching.

Bias Block

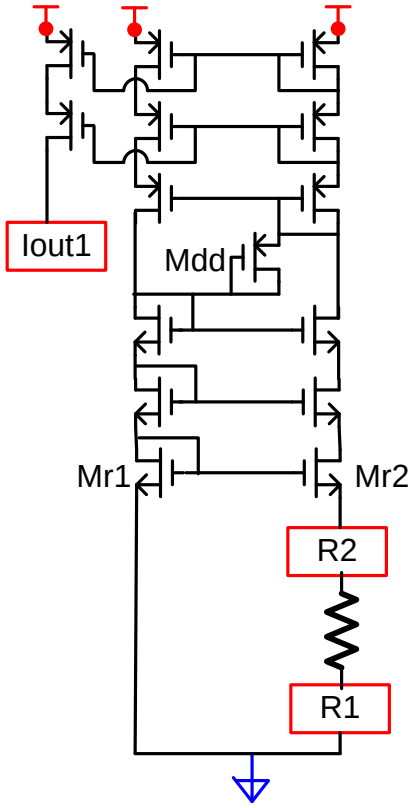

Figure 4.9 Current Bias Cell

Figure 4.9 shows a transistor level schematic of each of three current bias cells. They are for bias Iref, the desired cross-over current, I_range, the range of the current sense circuit, and the bias current for the rest of the linear regulator. A resistor is connected between R1 and R2 off-chip. Transistor Mdd makes sure that the operating point of the biasing cell is always conducting current. Once current is flowing in the cell, transistor Mdd will turn off.

4.4 Layout

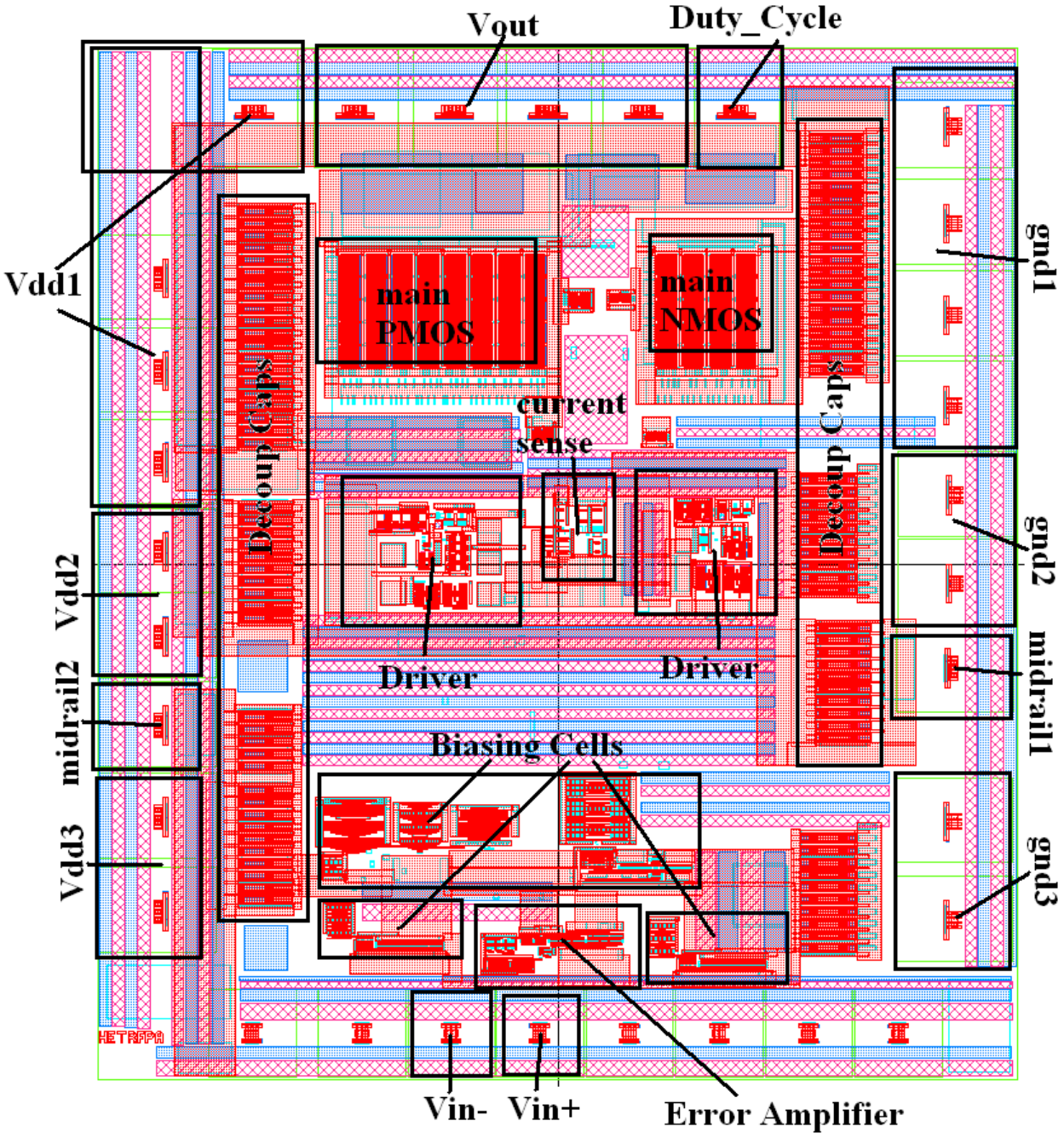

Figure 4.10 Layout of the Linear Regulator

Figure 4.10 shows the layout of the linear regulator. The technology is implemented in 0.18um CMOS, and the chip takes up 1mm by 1mm. The main PMOS transistor is 10mm and the main NMOS is 5mm. In order to satisfy the minimum transistor to substrate contact distance, the PMOS transistor is divided up into 40 identical blocks and NMOS is divided up into 20 identical blocks. The main PMOS (10mm) and its cascode (10mm) are identical sizes. Similarly, the main NMOS and its cascode are both 5mm. In order to minimize junction capacitors at node X in Figure 4.11, both NMOS and its cascode share on the same diffusion area. Figure 4.11 illustrates the layout concept.

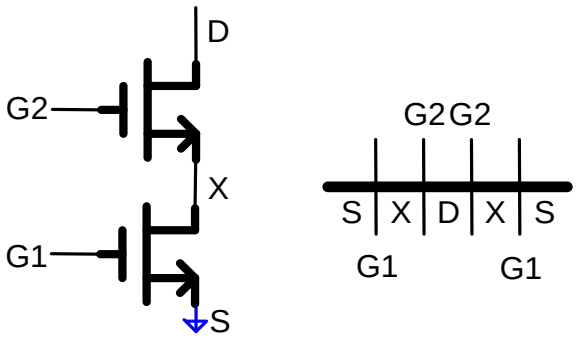

Figure 4.11 Stick Diagram of main NMOS and its Cascode

Figure 4.10 also shows that schematic supply symbols Vdd, midrail and gnd are separated into supply rails Vdd1, Vdd2, Vdd3, midrail1, midrail2, gnd1, gnd2, and gnd3. Separate rails are necessary to ensure that large currents flowing through the main PMOS and NMOS transistors do not interfere with the quiet bias part of the circuit. Supply rails Vdd1 and gnd1 are for main PMOS and main NMOS. Supply rails Vdd2 and gnd2 are the main PMOS transistor driver and the main NMOS transistor driver. Supply rails Vdd3 and gnd3 are for the error amplifier and the biasing current cells in the circuit. Supply rail Midrail1 is the midrail for the drivers and the main PMOS and NMOS transistors. Supply rail Midrail2 is the midrail for the

error amplifier and the biasing current cells. In addition, on-chip decoupling capacitors are placed to minimize voltage rail bouncing.

4.5 Simulation Results

Figure 4.12 shows a basic simulation setup for the linear regulator. A sample envelope signal is applied at signal Venv and the output voltage Vout drives the PA load, R_{load}. Current source I_{SR} models the current provided by the switching regulator. The crossover voltage would be I_{SR} x R_{load}. When the envelope signal Venv is equal to I_{SR} x R_{load}, the linear regulator provides zero current to the load. Current Ip is the current conducting in the main PMOS transistor and current In is the current conducting in the main NMOS transistor.

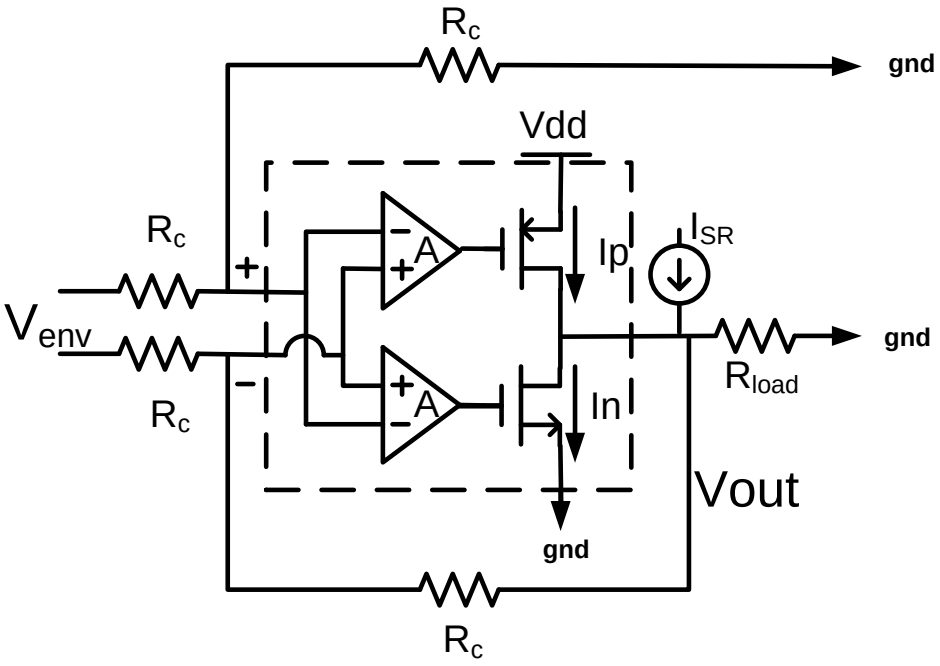

Figure 4.12 Linear Regulator Simulation Setup

Figure 4.13 shows the simulation results when the envelope voltage is a 2MHz sine wave with DC at 1.8V and amplitude = 1.6V. The crossover voltage is 1.8V. The load impedance that the linear regulator drives is 4Ω. The envelope signal and the output voltage are plotted on the fourth graph. Both signals overlap very well. The difference between Venv (or Vin) and Vout is Verr and is plotted on the first graph. Voltage error Verr is around 0V on average and peaks at 45mV whenever crossover happens. The 3rd graph plots the currents through the main transistors Ip and In. One can observe that for Venv above the crossover voltage, In is zero and the main PMOS transistor sources adequate current for tracking. Similarly, when Venv is below the crossover voltage, Ip is zero and the main NMOS transistor sinks adequate current for tracking. The second graph plots the linear regulator duty cycle. Whenever Ip is greater than In, duty_cycle is high. Whenever Ip is less than In, duty_cycle is low.

The linear regulator is also tested under a sample 802.11g envelope waveform. Figure 4.14 plots the envelope signal Venv and the output voltage Vout when driving a PA load. The error difference is plotted on the second graph. The average error is around 0V and has a peak of 70mV. The third graph plots the main PMOS transistor current and the main NMOS transistor current. Whenever the PMOS transistor turns on strongly, the main NMOS transistor turns off and vise versa. The last graph plots the linear regulator duty cycle. The error difference peaks during crossover. This is because when current in the main transistors during crossover is low and therefore causes a low transconductance Gm value. This reduces the loop gain thereby increasing the voltage error.

Figure 4.15 plots the crossover current in the main PMOS transistor and in the main NMOS transistor as the desired crossover current command is swept. As the current command increases, the actual crossover current also increases. However, there is an offset in the graph.

When the command current is 0, the actual crossover current is 5mA. This offset can be explained by the drain-to-source voltage Vds matching difference in the main PMOS and in the mirror replica. When main PMOS transistor is conducting 10mA, it is operating under weak inversion. Under weak inversion, current is sensitive to Vds voltage. Due to Vds mismatch, that creates an offset. Of course, we can always tune the command and measure the actual current.

Figure 4.16 plots the crossover current versus the crossover voltage when the desired current command is set to be 10mA. One can see that the PMOS and NMOS crossover currents are insensitive with respect to the crossover voltage. This shows that the minor loop is working.

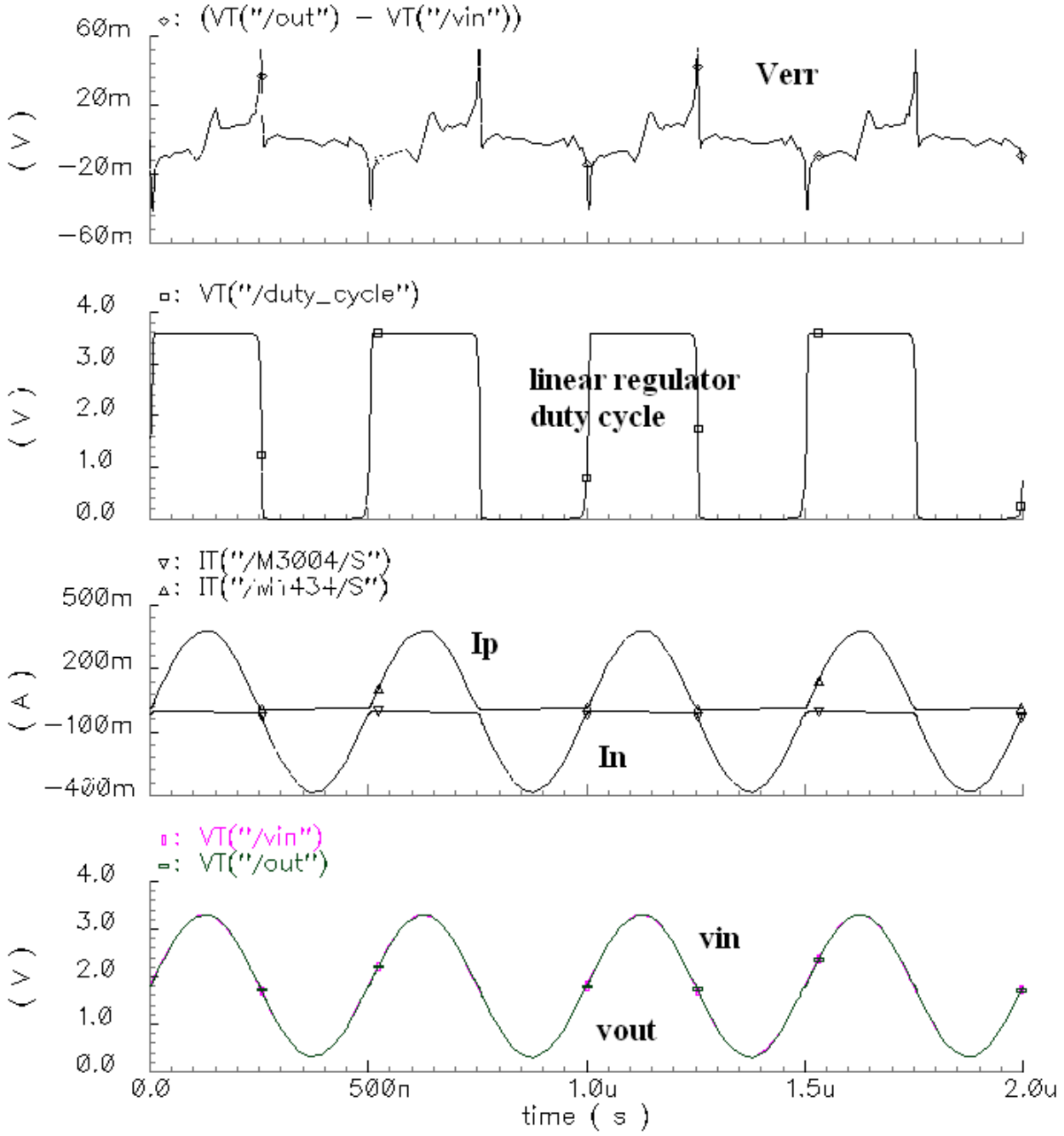

Figure 4.13 1st: Vout and Vin difference, 2nd: Linear regulator Duty Cycle, 3rd: main PMOS current and main NMOS current, 4th:Vin and Vout

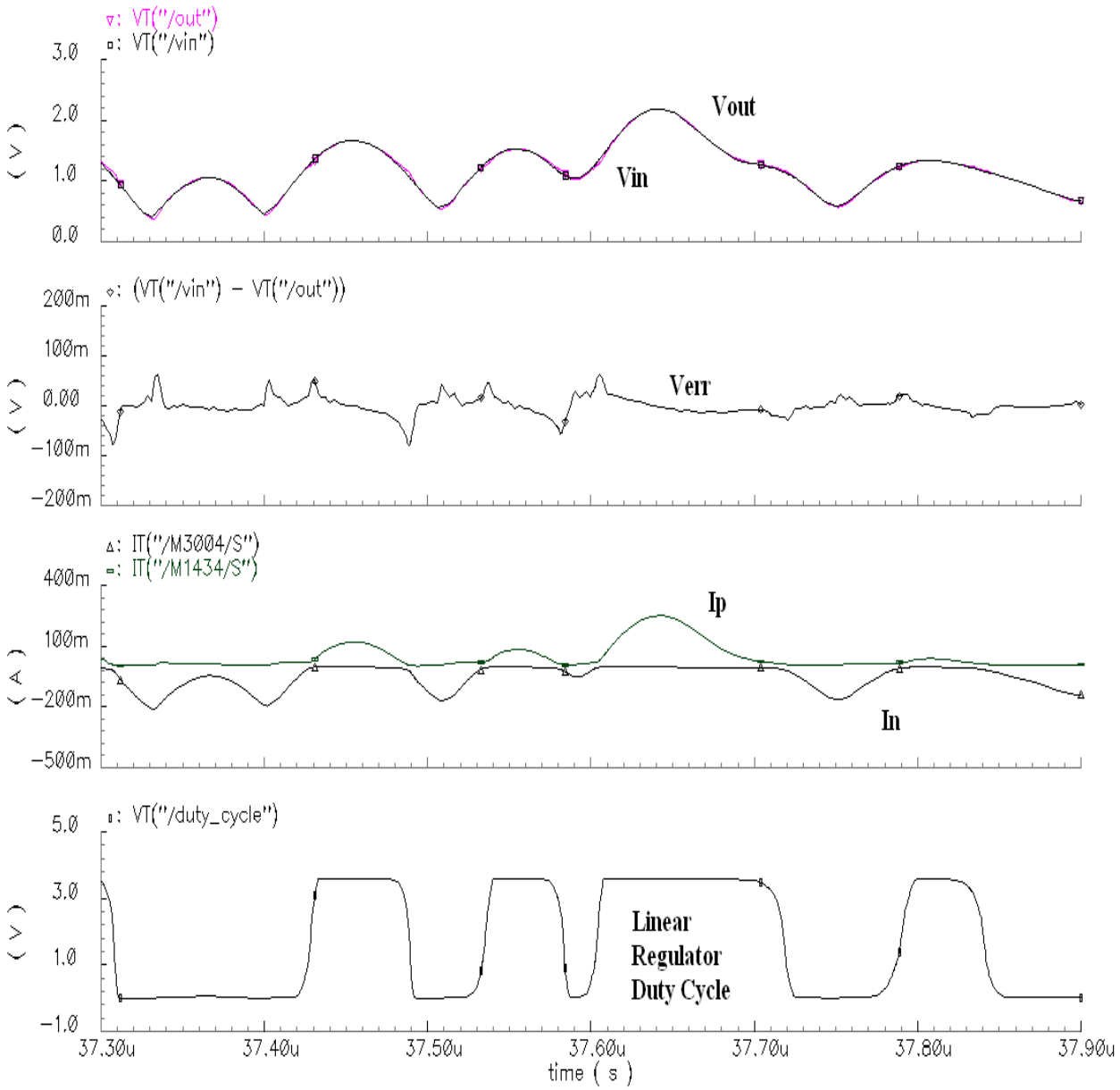

Figure 4.14 1st: Vin and Vout, 2nd: Vin and Vout difference, 3rd: current of main PMOS and main NMOS, 4th: Linear Regulator Duty Cycle

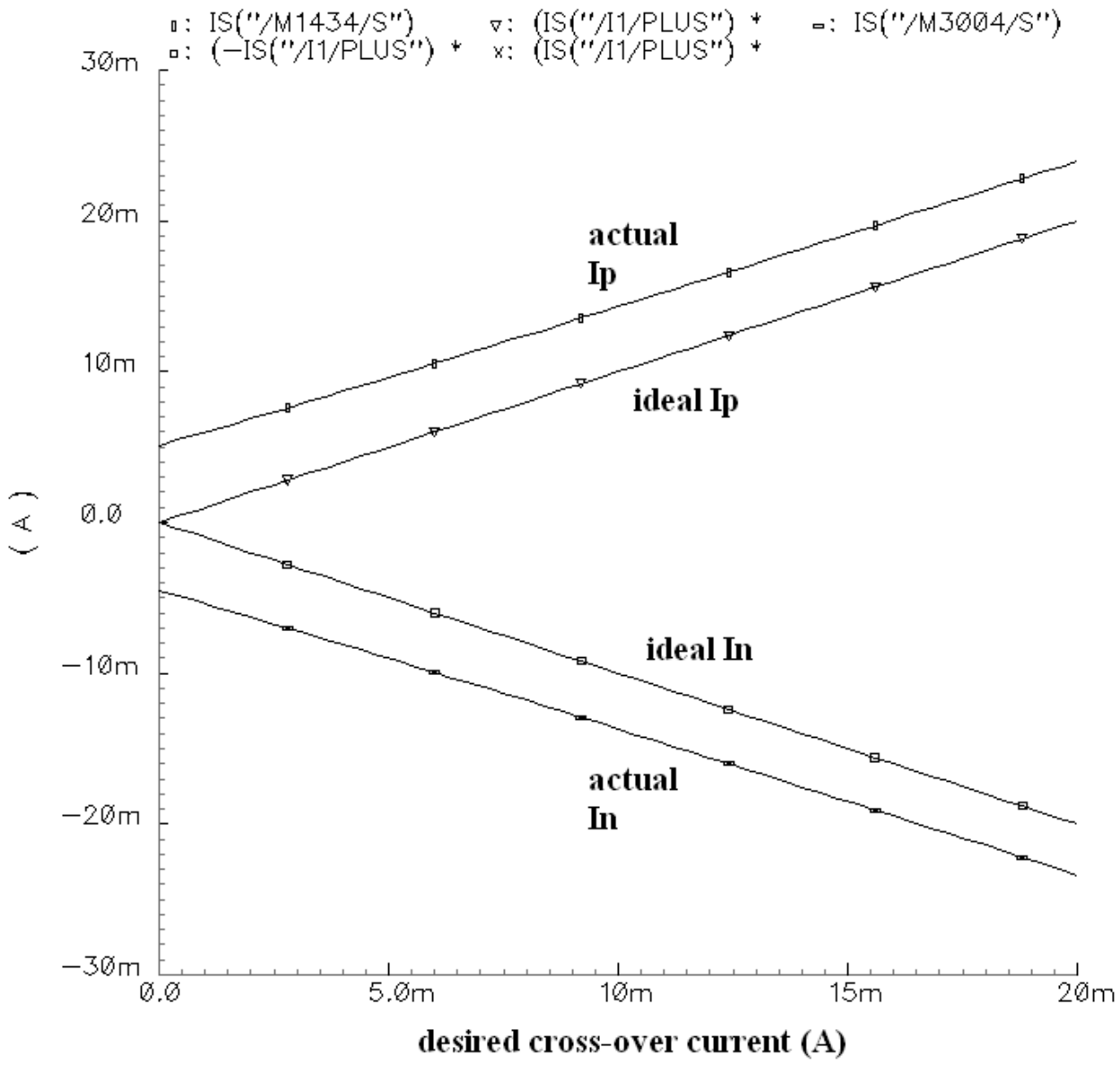

Figure 4.15 Actual main PMOS current and NMOS current versus crossover current command at crossover point

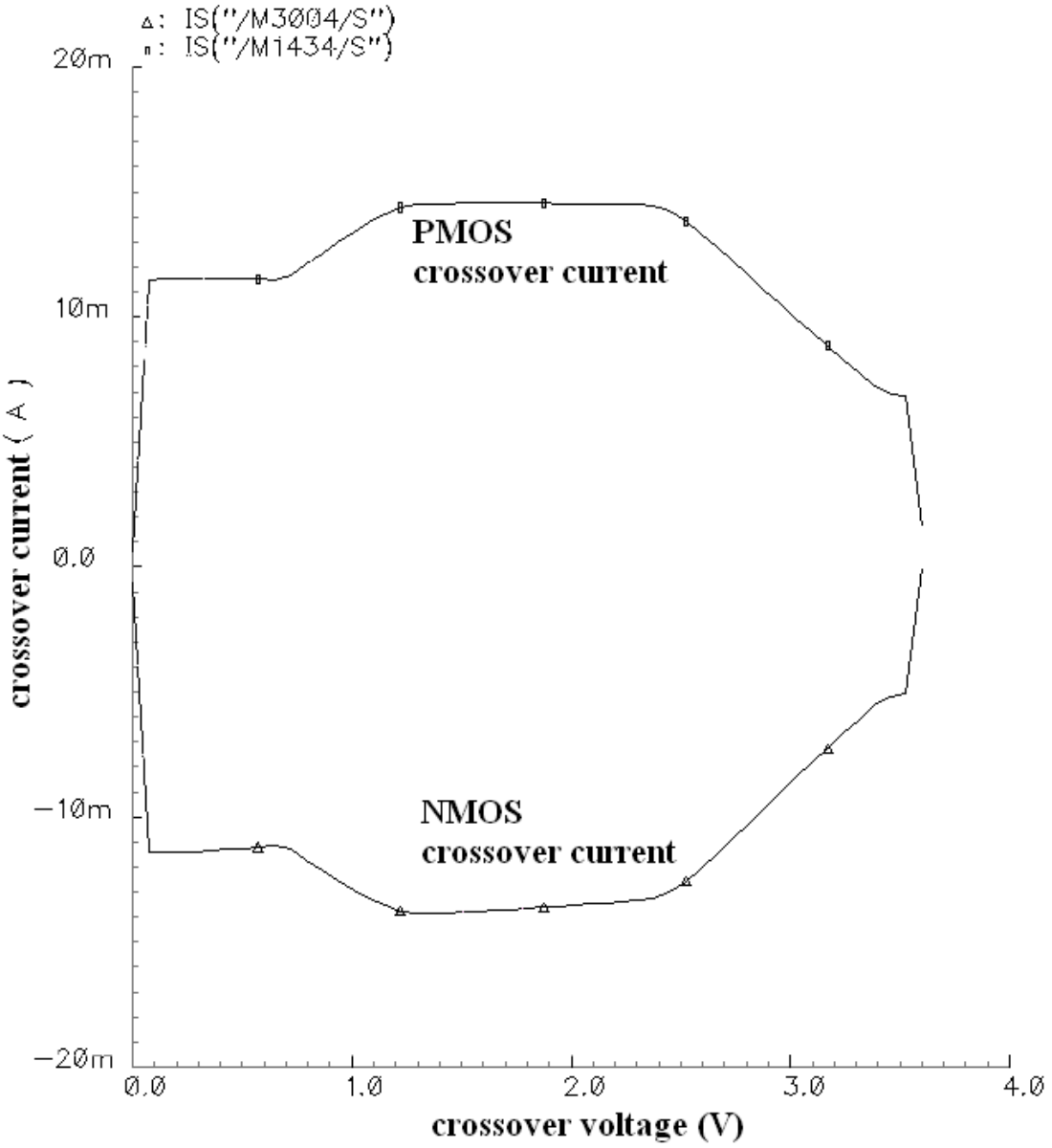

Figure 4.16 main PMOS and NMOS current versus output voltage

Desired $I_{crossover}$ = 10mA

Chapter 5

Conclusion

The purpose of this report is to improve the efficiency of dynamic supply regulator for RF PAs. Since supply regulators provide the majority of power to the PA, efficiency of supply regulators is crucial in achieving high overall efficiency. Specifically this project mathematically analyzes the efficiency of a parallel hybrid linear switching regulator. The analysis assumes that the only source of energy loss comes from the sourcing and sinking mechanisms of the linear regulator. It was shown that the highest efficiency is obtained when the linear regulator duty cycle is equal to the average envelope signal normalized by Vdd. A new efficiency optimization architecture is proposed. Here the linear regulator duty cycle tracks the average envelope signal normalized by Vdd by varying the switching regulator current. Simulations are made in Matlab Simulink to verify the theory.

The second part of this report is the design of a linear regulator. The linear regulator is designed to track the envelope signal of a sample 802.11g waveform. It is designed for Vdd = 3.6V in 0.18um CMOS. It has the ability to sink and source 500mA of current. Furthermore, it is designed to have a gain-bandwidth product of 300MHz. A minor loop is designed to control the crossover current. Transistor level simulations are made to verify both the tracking ability and the crossover current control ability of the linear regulator.

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